TM-011

GRAND TRAK 10

& TRAK 10

Service Information
(PCB Logic)

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1. GENERAL MAINTENANCE INFORMATION

1-1. INTRODUCTION

1-2. Gran Trak 10 is a new type of video game, and the operation of the new circuitry must be learned before your troubleshooting attempts will be successful. However, after the basic differences are understood, it should prove no more difficult than any other Atari printed circuit board (PCB) computer. The main differences between GT-10 and previous Atari games are the steering circuitry, the hybrid chips, the ROM (read only memory) and the power supply.

1-3. The steering circuitry is a novel bit of engineering which employs phototransistors and infrared light emitting diodes to generate pulses indicating the direction of steering wheel rotation. Fortunately, it is quite a simple circuit and easy to troubleshoot.

1-4. The hybrids are three custom chips which have been specially manufactured for this game. Troubleshooting these chips involves only verifying the correct input/output conditions and replacing the chip if the output conditions are not correct.

1-5. The ROM is another chip which has been specially programmed for GT-10 and it is used to generate the information for the display of the car, the score and game timer and the race track. Troubleshooting the ROM is probably one of the easiest tasks because it involves only unplugging the suspected chip and replacing it with a known-to-be-good ROM.

1-6. The power supply is more complicated because additional voltages are needed to operate the ROM, the hybrids and the on-board audio amplifier. Even though there are a few more voltages to check, the basic power supply troubleshooting methods remain unchanged.

1-7. TEST EQUIPMENT

1-8. Because of this new circuitry, more test equipment is required to check the PCB. An oscilloscope is an absolute necessity and a logic comparator would be a wise investment.

1-9. Some of the following instruments are absolutely essential to fully test the GT-10 PCB; others are desirable because they make the test procedures easier, but are not essential. Many of these items are available from the Atari Customer Service Department, and these items are indicated by an asterisk (*). A few others are available only from electronics supply houses or rental agencies; however, if you have difficulty in obtaining any needed instrument, contact Atari Customer Service for assistance.

1-10. **Required Equipment:** Atari recommends the following as a minimum set of test equipment:

a. **Logic Probe*:** The logic probe is an instrument designed for checking the outputs of integrated circuits. Atari recommends the Kurz-Kasch Logic Probe, model No. LP-520. The logic probe will indicate if a signal is a logic high, low or changing from one state to the other. Consult the operating instructions included with the unit for further details on its operation.

b. **Video Probe*:** The video probe is a simple, but useful testing device. It consists of two IC test clips (or one clip and a test prod), a length of wire and a 4.7K, 1/4W carbon resistor. Video probes may be obtained free of charge from the Atari Customer Service Department, or, if necessary, they can be assembled from standard parts available at any electronics supply house. To use the video probe, attach one clip to the negative side of the video coupling capacitor (C44) and clip or touch the other end to the desired signal test points as indicated in the following pages. The VP will display the signal directly on the CRT.

c. **The Oscilloscope:** The oscilloscope is used for viewing various waveforms. The application requires at least a 50 MHz scope and a dual trace unit to facilitate comparison between waveforms is desirable. Atari's specific recommendation is the Tektronix model No. 465, 100 MHz dual trace oscilloscope.

d. **Atari Universal Test Fixture:** The Atari Universal Test Fixture can be used to test the computer boards for Pong, Pong Doubles, Super Pong, Rebound, Space Race, Gotcha, and Quadrapong. This test fixture is equipped with a 12 inch TV monitor, two 5 volt BNC connectors for use where a regulated 5 volt source is required, and all the controls necessary to operate the computer boards. Connector cables must be ordered separately for each different type of PCB to be tested. The test fixture and cables are only available through the Atari Customer Service Department.

1-11. Optional Equipment: The following pieces of test equipment are not essential but will make your troubleshooting easier.

a. **The Logic Comparator*:** This compact troubleshooting instrument will prove invaluable in verifying correct IC operation. The unit simply clips onto in-circuit ICs and instantly displays any logic state difference between the in-circuit test IC and the reference IC in the comparator. Logic differences are identified to the specific pin by a lighted LED. If this instrument is purchased from the Atari Customer Service Department, it will be shipped with 20 pre-programmed reference boards. If the instrument is purchased elsewhere, you will have to program the boards yourself. Atari recommends either the Hewlett Packard 10529A comparator or the Fluke comparator.

b. **The Logic Pulser*:** The logic pulser is used to stimulate in-circuit ICs so they are driven to their opposite states and we recommend the Hewlett Packard 10526T pulser.

1-12. TROUBLESHOOTING SUGGESTIONS

1-13. The first step in the troubleshooting process is to correctly identify the observable symptoms of the malfunction and then to narrow down the possibly malfunctioning areas as much as you can. This should reduce the situation to one or two functional blocks which might be at fault. Then start examining these functional blocks with your test instruments and compare the results with the operational analysis and test point information under the heading of that functional block. Keep in mind, however, that the first observable symptoms of a malfunction are not necessarily due to the functional block which produced those symptoms. A failure in one part of the PCB may affect much, if not all, of the PCB.

1-14. Some malfunctions may produce symptoms which are not clearly attributable to one component. Sync problems can be especially nasty in this regard because you can spend quite some time verifying the presence of correct sync signals on the board only to discover it is the monitor which is distorting sync.

1-15. For these problems, use substitution as a troubleshooting technique. For instance, to clearly identify which component is at fault in a sync problem, try substituting a known-to-be-good TV monitor. If you have built a test fixture, plug the suspected board into the fixture and if the sync problem disappears, the other TV must have been the cause. Conversely, had the problem not disappeared, the substitution test would have revealed a malfunctioning board and you would begin the troubleshooting process at the sync section.

1-16. The same technique can be used to test the Read Only Memory (ROM) which is inserted in a plug-in type receptacle to facilitate the substitution test. If you have a problem with the car image, the race track display or the score or timer displays, try inserting another and known-to-be-good ROM and if this clears up the malfunction, leave it there. However, we must note that the ROM failure rate has been extremely low so it is more likely that a display problem is located in either the ROM address circuitry or the display circuits.

1-17. There are a few other problems which need mentioning because, while they may at first appear to be board related, closer examination will reveal they are location related. If the ac line voltage fluctuates enough, the electronic latch will turn off game credit. One cause of this may be a large load connected to the same line as the machine. For example, a large air conditioner while starting up may drop the line voltage enough to break the electronic latch. Another cause may be that the line voltage drops at certain peak times of the day (e.g., dusk). Local ac power is suspect in any malfunction which occurs on an intermittent basis.

1-18. Another game credit problem which may be either constant or intermittent in nature is a maladjusted antenna wire. The antenna wire is connected to the electronic latch and, if the wire is too long, game credit may be accidentally turned off, especially if the machine is in a carpeted location.

1-19. PCB ADJUSTMENTS

1-20. Most of the PCB adjustments are quite simple and only involve changing a slide switch to the desired position or adjusting a small blue trim pot "by ear". A few others, however, are more complex and require an oscilloscope or, preferably, a frequency counter. This section contains only the adjustment procedures; consult the text for a fuller understanding of how these adjustments affect their associated circuits. See Figure 2-32 for the location of the PCB adjustments.

a. **Test Switch:** While you are testing the PCB, you may wish to set this switch to the TEST position which will freeze the game timer and disable the crash mode. Always return the switch to the PLAY position before placing the PCB back in operation.

b. 1P-2P Switch: If this switch is set to the 1P position, the player will receive one game per each coin he deposits; if set to the 2P position, he will receive two games.

c. Volume Adjustment: This pot controls the gain of the audio amplifier. Adjust the volume to the preference of the location, and keep in mind that the machine will sound louder with the door off.

d. Play Time Adjustment: This pot controls both the total game length and the crash time period. The play time counter (to the right of the lap score in the pit area) always begins counting down from 78 by 2's. Adjusting the play time pot causes the game counter to count down slower or faster. Adjusting for a longer game will also increase the length of the crash time, and affect score interpretation per the "rating card" posted on front of the CRT.

e. Speed Adjustment: This adjustment controls the maximum velocity of the car. You must have either a logic probe or an oscilloscope to perform this adjustment. Attach the probe to B2-9 and adjust the pot until the signal ($\overline{1\ STOP}$) goes completely high when the car is traveling at maximum speed in third gear.

f. "A" Adjustment: You must have an oscilloscope or a frequency counter to adjust the following three engine sounds (A, B & C). Clip the test instrument to C8-3 (the square wave output pin) and adjust the A pot for a 13 ms square wave or a frequency counter reading of 73 Hz.

g. "B" Adjustment: Clip test instrument to D8-3 and adjust the pot for a 3.07 ms square wave or a frequency of 325 Hz.

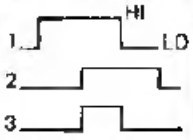
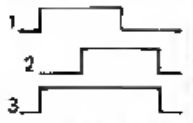
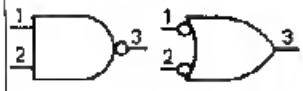
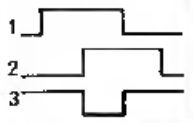
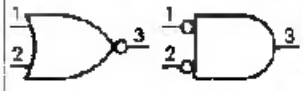
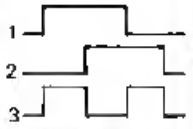
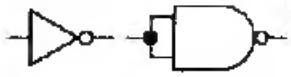
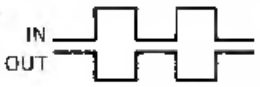
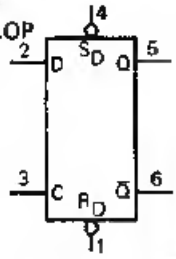
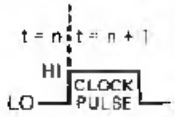
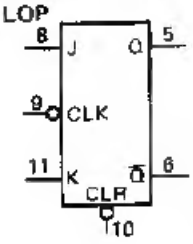
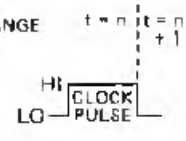
h. "C" Adjustment: Clip test instrument to E8-3 and adjust the pot for a 7.42 ms square wave or a frequency of 412 Hz.

i. Screech Adjustment: This pot adjusts both the screech and crash sounds simultaneously. Adjust the pot by ear for the best sound output.

1-21. LOGIC SYMBOLOGY

1-22. Table 1-1 describes the operation of the most common logic circuits found on the computer board. Those not covered in the table are explained at their first appearance in the computer board circuit description in Section 2. Logic circuits are identified in the text and on the schematic by their actual grid location on the PCB and their output pin number (e.g., gate A6-3 would be the gate with output pin 3 in the logic package at location A6 on the PCB). The logic levels on the PCB are 0 to +0.4 volts for LO and +2.6 to +5 volts for HI. Signal names overscored (e.g., $\overline{START}$ and pronounced "start not") go LO to initiate events and those not overscored go HI when active. Overscored signals are always at the logic level opposite to that of their non-overscored counterparts (i.e., $\overline{START}$ is always at a logic level opposite to START).

Table 1-1. Logic Symbology

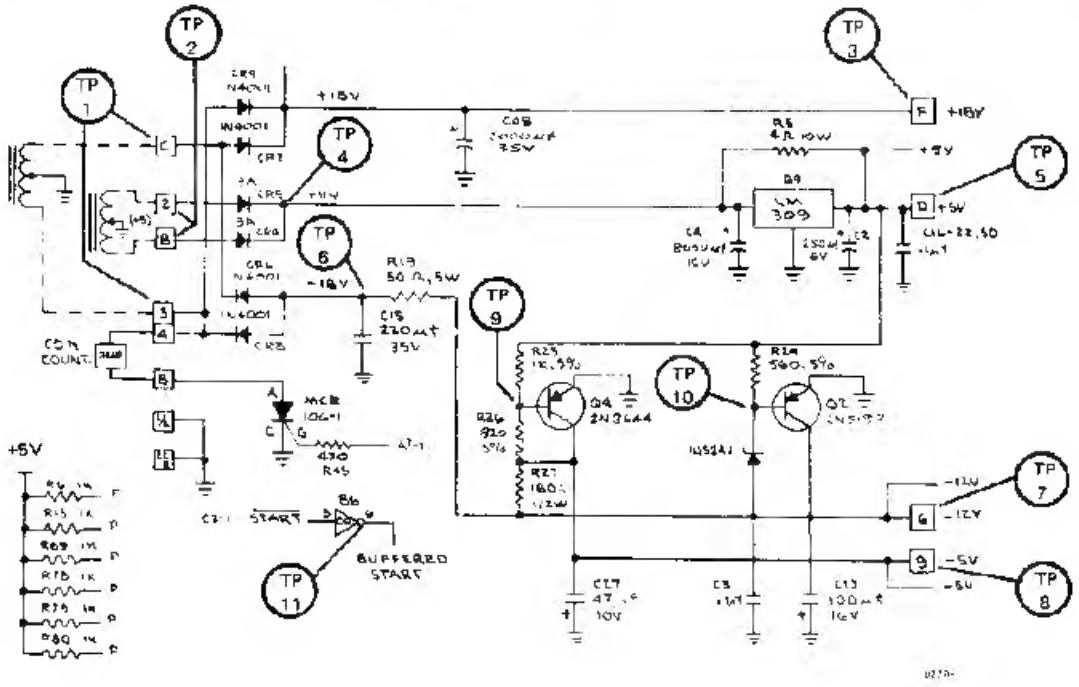
SYMBOL	TRUTH TABLE/TIMING	OPERATION
AND GATE 	1 2 | 3 LO LO | LO LO HI | LO HI LO | LO HI HI | HI 	Output is HI only when all inputs are HI, otherwise output is LO. Rule applies for any number of inputs.
OR GATE 	1 2 | 3 LO LO | LO LO HI | HI HI LO | HI HI HI | HI 	Output is HI when any input is HI. Output is LO only when all inputs are LO.
NAND GATE 	1 2 | 3 LO LO | HI LO HI | HI HI LO | HI HI HI | LO 	Output is LO only when all inputs are HI, otherwise output is HI.
NOR GATE 	1 2 | 3 LO LO | HI LO HI | LO HI LO | LO HI HI | LO 	Output is LO when any input is HI. Output is HI only when all inputs are LO.
EXCLUSIVE OR GATE 	1 2 | 3 LO LO | LO LO HI | HI HI LO | HI HI HI | LO 	Output is HI when either but not both inputs are HI, otherwise output is LO.
INVERTERS 		The 2-input NAND or NOR gate can be used as inverters by tying one input to a fixed level or tying both inputs together.
D-TYPE FLIP-FLOP 	t = n t = n + 1 D Q | Q LO LO | LO LO HI | LO HI LO | HI HI HI | HI  Truth Table valid only when S_D and R_D are both HI	When both S_D (direct set) and R_D (direct reset) are HI, level at input D is transferred to output Q when input C (clock) goes HI. A LO on S_D forces Q HI and $\overline{Q}$ LO. A LO on R_D forces $\overline{Q}$ HI and Q LO. S_D and R_D predominate over all other inputs.
J-K MASTER SLAVE FLIP-FLOP 	t = n t = n + 1 J K Q | Q Q LO LO – | NO CHANGE LO HI – | LO HI HI LO – | HI LO HI HI LO | HI LO HI HI HI | LO HI  Truth Table valid only when CLR is HI	When CLR is HI and: 1. J and K are both LO, clock pulse has no effect on outputs Q and $\overline{Q}$. 2. J and K are at opposite logic levels, negative-going clock edge transfers J level to Q and K level to $\overline{Q}$. 3. J and K are both HI, each negative-going clock edge alternates outputs Q and $\overline{Q}$. 4. LO on CLR forces and holds Q LO and $\overline{Q}$ HI.

2. CIRCUIT DESCRIPTION

2-1. THE POWER SUPPLY

2-2. The power supply for GT-10 is a bit more complicated than in previous games because additional voltages are needed to operate new circuitry. The normal +5 volts is still used to power most of the ICs; however, the ROM requires -12 volts and the hybrids need -5 volts and -12 volts. The +18 volt source is used only to drive the audio amplifier.

2-3. The four circuits which generate the different voltages are very similar. See Figure 2-1. First, the 110 VAC line voltage is stepped down by the transformer(s) to 32 VAC and 16 VAC. These secondary voltages are then processed by the on-board power supply components to generate the DC supplies.



TP 1: OSCILLOSCOPE: 32 VAC
VOM/VTVM: 32 VAC

TP 2: OSCILLOSCOPE: 16 VAC
VOM/VTVM: 16 VAC

TP 3: OSCILLOSCOPE: + 18 VDC
VOM/VTVM: + 18 VDC

TP 4: OSCILLOSCOPE: + 11V PEAK
VOM/VTVM: + 8.5 VDC

TP 5: LOGIC PROBE: High
OSCILLOSCOPE: + 5 VDC
VOM/VTVM: + 5 VDC

TP 6: OSCILLOSCOPE: - 18 PEAK
VOM/VTVM: - 15.5 VDC

TP 7: OSCILLOSCOPE: - 12 VDC
VOM/VTVM: - 12 VDC

TP 8: OSCILLOSCOPE: - 5 VDC
VOM/VTVM: - 5 VDC

TP 9: OSCILLOSCOPE: - 0.6 VDC
VOM/VTVM: - 0.6 VDC

TP 10: OSCILLOSCOPE: - 1.0 VDC
VOM/VTVM: - 1.0 VDC

TP 11: LOGIC PROBE: High pulse when the start switch is operated.
OSCILLOSCOPE: High pulse when the start switch is operated.

Figure 2-1. The Power Supply and Buffered Start

2-4. **+5 Volts:** To create the regulated +5 volts needed by the ICs (and other components as well), the 18 VAC waveform at edge connector pins 2 and 8 is full-wave rectified by diodes CR4 and CR5. The resulting DC voltage is then filtered by capacitor C4 and then regulated to a constant +5 volts by the LM 309 voltage regulator.

2-5. **+18 Volts:** The 32 VAC waveform at pins 3 and C is rectified by CR7 and CR9, filtered by C49 and taken directly to the audio amplifier.

2-6. **-12 Volts:** Because the cathodes of CR8 and CR8 are wired to the transformer secondary, the resulting voltage will be negative with respect to ground. This waveform is filtered by C15 and then lowered to -12 volts by R19. The resulting voltage is regulated by transistor Q2 which acts like a shunt regulator to keep the voltage constant with respect to current.

2-7. **-5 Volts:** This circuit works similarly to the -12 volt circuit. Resistor R27 drops the -12 volts to -5 volts which is filtered by C27 and regulated by Q4.

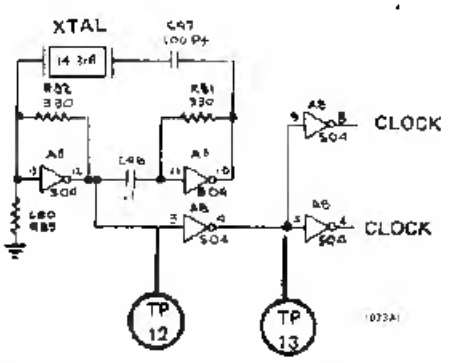
2-8. **The Pull-up Resistors:** The pull-up resistors (R6, R15, R69, etc. and denoted by the schematic symbol "P") are used to provide a logic high source for inputs to ICs which need to be tied high. The resistor limits the total current drain through the LM 309.

2-9. BUFFERED START

2-10. In order to prevent a high, and possibly destructive, inductive kickback when the coil of the game counter is de-energized, a buffered start circuit has been incorporated so that the game counter is now tripped by a silicon controlled rectifier (MCR 106-1). $\overline{\text{START}}$ is inverted by B6 and this output is connected to the gate input of the rectifier. When the signal goes high, the silicon controlled rectifier conducts, thereby energizing the coil of the game counter. On the next half-cycle of the AC current, the rectifier is shut off by the AC waveform and the coil is de-energized.

2-11. THE OSCILLATOR

2-12. Since the operation of the computer is synchronous, it requires a master timing signal which is provided by the oscillator and known as the CLOCK. See Figure 2-2. The crystal oscillator generates a 14.318 MHz clock and it is kept oscillating by two closed-loop amplifiers which consist of a 330 ohm, 1/4 watt feedback resistor and an inverter. These amplifiers are coupled together by a 0.1 uf capacitor (C46) and they operate out of phase with respect to each other. Inverter A8-4 is used as a buffer-amplifier and inverters A8-6 and A8-8 expand the oscillator's loading capacity. The clock signal is sinusoidal in form.



TP 12: LOGIC PROBE: High, low and pulsing.
OSCILLOSCOPE: 14 MHz sine wave.

TP 13: LOGIC PROBE: High, low and pulsing.
OSCILLOSCOPE: Same as TP 12, except out of phase.

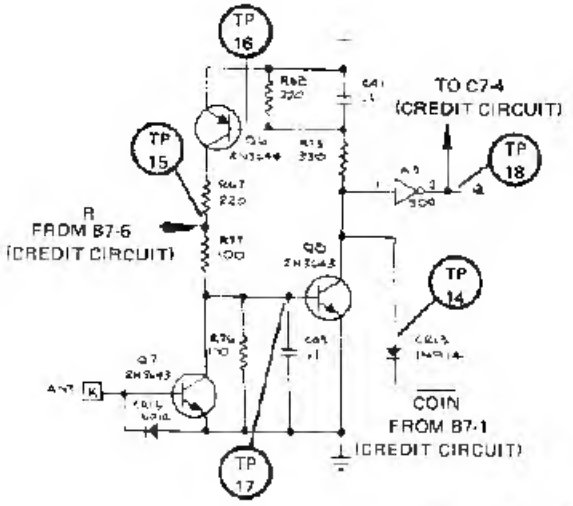
Figure 2-2. The Oscillator

2-13. THE ELECTRONIC LATCH

2-14. The electronic latch permits the starting of a new game when the coin is deposited and prevents the start of a game if the player attempts to obtain free game credit by inducing a static charge in the machine. See Figure 2-3 for the following discussion.

2-15. The control of game credit is accomplished by the presetting of the attract flip-flop C7-5 (see the credit and start circuit, Figure 2-4). Whenever the output of the latch circuit, signal Q, is high, the attract signal (ATRC) will also be high. If ATRC goes high, the computer is reset back to the ATTRACT mode and the game ends. In order for the game to begin, the electronic latch must be "latched" and signal Q must be low.

2-16. The latch cycle is started when $\overline{\text{COIN}}$ (the normally high output of the credit circuit) goes low as the coin is deposited. This low takes the base of transistor Q6 low which causes the collector of that transistor to go high. This, in turn, causes Q8 to turn on and its collector goes low. Since the collector of Q8 is tied to $\overline{\text{COIN}}$, it keeps the latch circuit low even after $\overline{\text{COIN}}$ returns high as the coin switch is released. The circuit is now said to be "latched" and will remain in the latched condition until shut off by a low R signal or a high antenna signal.



TP 14:	LOGIC PROBE:	High going low when coin switch is operated.
	OSCILLOSCOPE:	Same as Logic Probe.
TP 15:	LOGIC PROBE:	High during game and low at game over.
	OSCILLOSCOPE:	Same as Logic Probe.
TP 16:	OSCILLOSCOPE:	+5 volts until coin switch is operated; then drops to approximately +1 volt.
TP 17:	OSCILLOSCOPE:	0 volts until coin switch is operated, at which time it rises to + 8 volts and remains there until game over.
TP 18:	LOGIC PROBE:	High during game mode, low during attract mode.
	OSCILLOSCOPE:	Same as Logic Probe.

Figure 2-3. The Electronic Latch

2-17. R is the credit signal from B7-6 in the credit circuit. A low R drags the base of Q8 low and, since Q8 can no longer conduct, the latch cycle is broken. This toggles the attract flip-flop and resets the computer to the ATTRACT mode.

2-18. The same type of process is used to prevent players from gaining free game credit by inducing a static charge in the machine. When a large enough static charge is discharged to the machine, the antenna wire picks up the necessary current to create a high at the base of Q7. This causes Q7 to conduct and the low at its collector turns off Q8 and breaks the latch cycle.

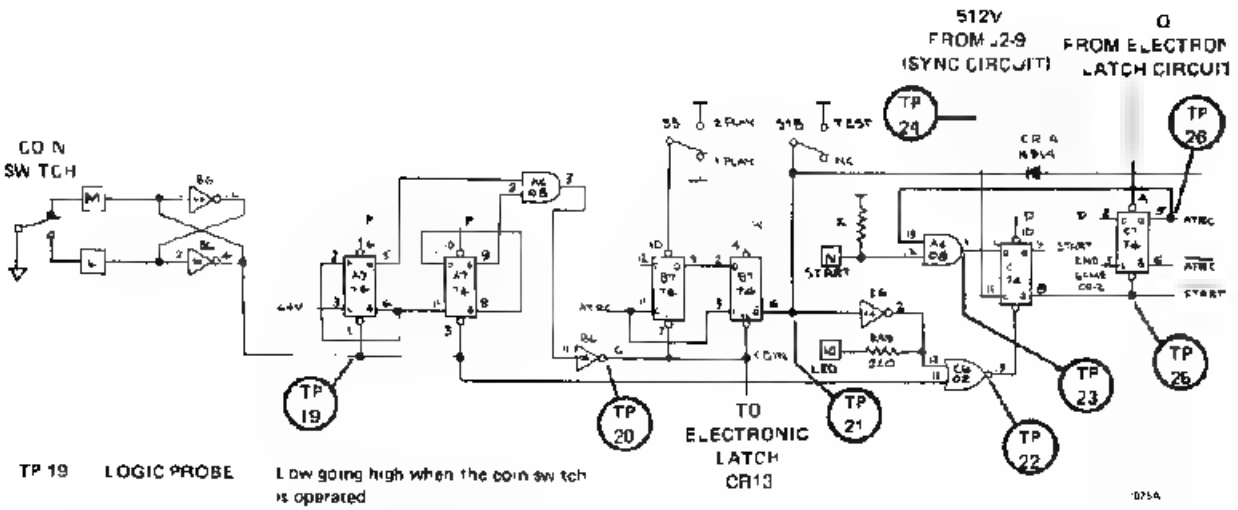
2-19. THE CREDIT AND START CIRCUIT

2-20. The credit portion of this circuit records the deposit of the coin and lights the credit lamp (LED). This provides game credit to the start circuit which is operated by the player to reset the PCB and begin the new game. The circuit is shown in Figure 2-4.

2-21. The deposited coin closes the normally-open side of the coin micro-switch, and the outputs of this switch are inverted by a debouncing circuit consisting of the two B6 inverters. The debouncing circuit eliminates undesired impulses created by the chattering of the coin switch contacts. The debouncing circuit outputs enter the clear inputs of flip-flops A7. These two flip-flops constitute an anti-cheat device, designed so that incidental or player-induced vibrations which may operate the coin switch trip wire will not produce game credit. In order to get the correct outputs from the A7 flip-flops, the coin switch contacts must make for at least 128 horizontal sync pulses, or about 9 milliseconds. Since most incidental or player-induced vibrations produce a coin switch make of only a few microseconds, the Q outputs of the flip-flops will not go high and no game credit will result.

2-22. However, if a coin is deposited, both A7 flip-flops are enabled, and when both of the Q outputs are high, pin 3 of AND gate A6 will also go high. This produces a low at pin 10 of inverter B6 which clears both B7 flip-flops. If the 1P/2P switch (1 play or 2 plays per coin) is set to the 1P mode, the preset input (pin 10) of B7 is held low and when $\overline{\text{COIN}}$ returns high, a high will appear at the Q output (pin 9) of B7. However, if the switch is set to the 2P position, when $\overline{\text{COIN}}$ goes low, the Q output (B7-9 will go low and stay low until the high at the D input (B7-12) is clocked through by the ATRC signal. A low also appears at the Q output (B7-6) which is inverted at B6-2 and lights the credit LED. The same signal which cleared the B7 flip-flops ($\overline{\text{COIN}}$) also drags the collector of transistor Q8 low and turns on the electronic latch (see Figure 2-3) which enables the attract flip-flop C7 at pin 4. Since the credit lamp must be lighted to enable gate C6, and since C6 enables the start flip-flop C7, the game cannot be started unless the credit lamp is lighted.

2-23. When the START switch is operated, pin 12 of AND gate A6 is pulled high by its 1K pull-up resistor, and since the ATRC line (A6-13) is already high, pin 11 of A6 will go high. This produces a high at the D input of start flip-flop C7 at pin 12. Since the clock input of this flip-flop is connected to vertical sync at 512V (J2-9), the high at the D input will be clocked out when 512V goes high and this is the START signal. Meanwhile, $\overline{\text{START}}$ goes low and



TP 19	LOGIC PROBE	Low going high when the coin switch is operated
	OSCILLOSCOPE	Same as Logic Probe
TP 20	LOGIC PROBE	High before coin switch is operated and high-low and pulsing while switch is held in the operated position.
	OSCILLOSCOPE	High before coin switch is operated and high with low-going pulses 4.6 ms wide occurring every 12.5 ms while coin switch is held in the operated position.
TP 21	LOGIC PROBE	Low before coin switch is operated and high thereafter until game over
	OSCILLOSCOPE	Same as for Logic Probe
TP 22	LOGIC PROBE	Low going high when coin switch is operated.
	OSCILLOSCOPE	Same as Logic Probe
TP 23	LOGIC PROBE	Low going high when the start switch is operated. Stays high during game
	OSCILLOSCOPE	Same as Logic Probe.
TP 24	LOGIC PROBE	Low and pulsing
	OSCILLOSCOPE	High pulses 0.28 ms wide occuring every 16.7 ms.
TP 25	LOGIC PROBE	High with a low going pulse when the start switch is operated
	OSCILLOSCOPE	Same as Logic Probe, except note that the low-going pulse is about 15 ms
TP 26	LOGIC PROBE	High during attract mode and low during game mode.
	OSCILLOSCOPE	Same as Logic Probe.

Figure 2-4. The Credit and Start Circuit

clears C7 at pin 1. This produces a low at the attract flip-flop output which returns to shut off gate A6 at pin 13, thereby starting the game and locking out the start switch so the player cannot reset the computer during the game and gain additional time.

2.24. TV MONITOR OPERATION

2.25. It is important that you understand the basics of TV monitor operation so that you can later comprehend how the signals generated by the PCB computer are synchronized with the operation of the monitor. We will not dwell on how the monitor receives and displays the information other than to say the electron beam illuminates spots on the phosphorescent coating of the CRT per the PCB signal information. What is critical is how these PCB signals are timed with the operation of the electron beam.

2.26. This type of TV monitor directs its electron beam in a fashion known as true interlaced raster scan. The TV screen picture (or raster) is composed of 260.5 horizontal lines stacked on top of one another. The electron beam always scans this raster whether or not it is receiving any PCB signals. The PCB signals simply modulate the electron beam so that spots of different intensity are illuminated. To see what this raster looks like, disconnect the PCB edge connector and turn the monitor brightness all the way up. The pattern of horizontal lines you see is the raster.

2.27. The electron beam begins its sweep in the top left hand corner of the CRT and sweeps one horizontal line which ends at the right-hand side of the CRT. The electron beam is then repositioned at the left-hand side of the CRT prior to sweeping the next line. The process of moving the beam from the right side back to the left is known as hor-

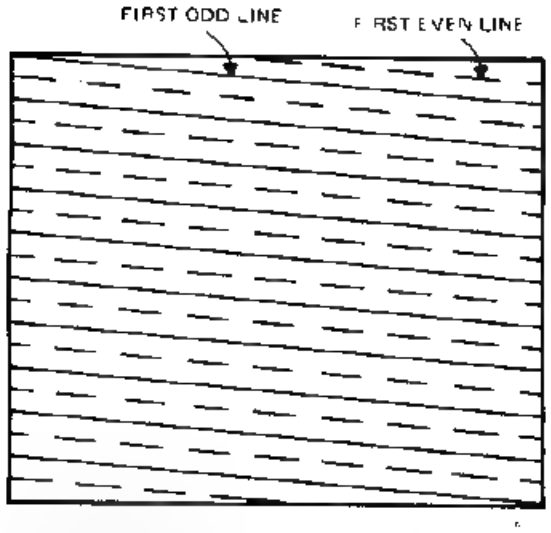


Figure 2-5. Interlaced Raster Scan

zontal retrace and the beam must be blanked out (horizontal blanking) during retrace so no undesired illumination occurs.

2-28. The electron beam skips the second line, sweeps the third, is blanked out, sweeps the fifth line and so on. When the beam has swept all the odd numbered lines it is said to have completed one odd field. After completing the odd field the beam is in the bottom right corner of the CRT. In order to begin the even sweep, it must be repositioned in the top center of the CRT where the first even line begins. The process of moving the beam vertically to the top of the screen is known as vertical retrace and, of course, the beam must be blanked out (vertical blanking) during vertical retrace.

2-29. The beam sweeps a full field of all the even numbered lines in the same fashion as it completed the odd field. This system of sweeping the odd lines first and then the even lines is known as interlacing. Two completely interlaced fields (one even and one odd) constitute one full frame. The electron beam sweeps the CRT at the rate of 30 frames per second.

2-30. SYNCHRONIZATION AND BLANKING

2-31. A complex system of synchronization is required so the video signals generated by the PCB computer modulate the electron beam when the beam is in the correct part of the CRT. The essence of synchronization is timing. When sync is malfunctioning, the images appear to shift and move about the CRT because they are displayed in a different place each frame. The PCB signals must synchronize with the electron beam horizontally so that the information on each line is displayed in the proper sequence (and also vertically so that the vertical positioning of the images is correct). The sync pulses "tell" the electron beam when to start and stop its sweep, but do not otherwise control the raster. The sync circuit signals are also used in many other places in the PCB to time other operations with the TV monitor.

2-32. The basic timing for the horizontal sync circuit is the clock frequency. Vertical sync, however, runs off of horizontal sync. The horizontal and vertical sync counters count down the clock pulses to form timed pulse trains (see Figure 2-6). The electron beam begins its sweep when horizontal reset (H RESET) goes low. This occurs after 451 clock pulses are counted out by the horizontal sync counters. The rising edge of the next H RESET pulse occurs

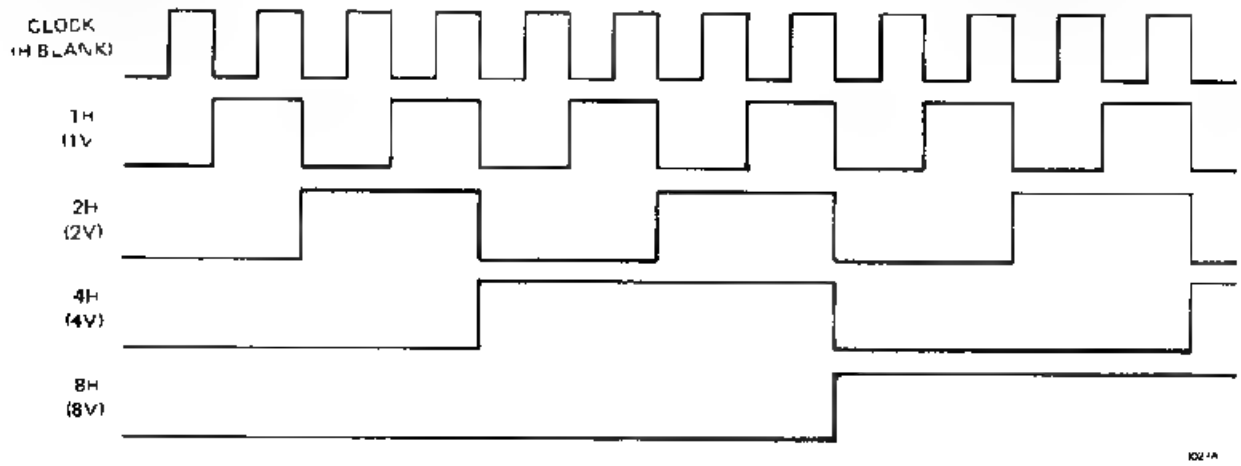
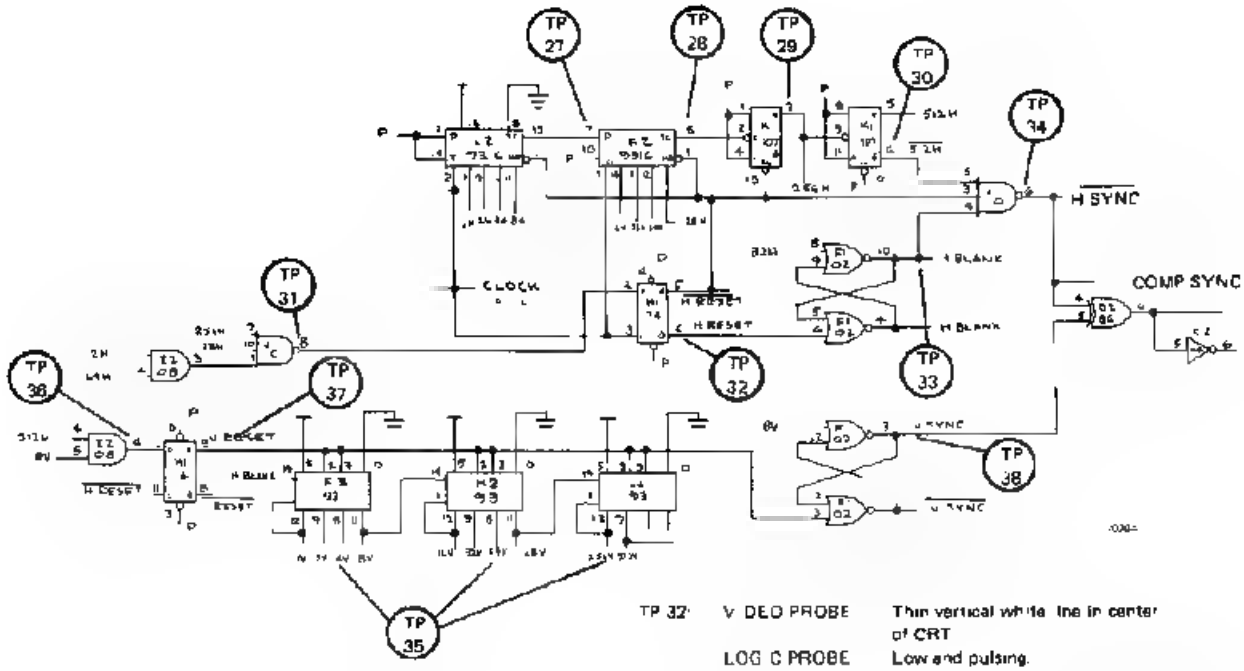


Figure 2-6. Sync Pulse Trains



TP 27	VIDEO PROBE	A number of thin vertical white lines.
	LOGIC PROBE	Low and pulsing.
	OSCILLOSCOPE	High pulses 0.07 ms wide and occuring every 1.12 ms.
TP 28	VIDEO PROBE	Two vertical white bands.
	LOGIC PROBE	Low and pulsing
	OSCILLOSCOPE	High pulses 1.3 ms wide and occuring every 32 ms.
TP 29	VIDEO PROBE	Alternating black and white bands.
	LOGIC PROBE	High, low and pulsing.
	OSCILLOSCOPE	Low pulses 14 ms wide and occuring every 32 ms
TP 30:	VIDEO PROBE	Left half of CRT black, right half white
	LOGIC PROBE	High, low and pulsing.
	OSCILLOSCOPE	Symmetrical square wave with a 64 ms period.
TP 31	VIDEO PROBE	One thin vertical black line in center of CRT
	LOGIC PROBE	High and pulsing.
	OSCILLOSCOPE	Low pulses 0.1 ms wide and occuring every 32 ms.
TP 32:	VIDEO PROBE	Thin vertical white line in center of CRT
	LOGIC PROBE	Low and pulsing.
	OSCILLOSCOPE	High pulses 0.1 ms wide and occuring every 32 ms.
TP 33	VIDEO PROBE	White vertical band in center of CRT
	LOGIC PROBE	Low and pulsing.
	OSCILLOSCOPE	High pulses 2.3 ms wide occuring every 33 ms.
TP 34	LOGIC PROBE	High and pulsing
	OSCILLOSCOPE	Low pulses 2.3 ms wide occuring every 64 ms
TP 35:	VIDEO PROBE	Starting with 2V, touch probe to all outputs up to 512V. Notice that the horizontal black and white bars double in width at each successive division.
TP 36:	LOGIC PROBE	Low and pulsing
	OSCILLOSCOPE	High pulses 20 ms wide occuring every 16.7 ms.
TP 37	LOGIC PROBE	Low and pulsing
	OSCILLOSCOPE	High pulses 30 ms wide occuring every 16.7 ms.
TP 38	LOGIC PROBE	Low and pulsing
	OSCILLOSCOPE	High pulses 0.25 ms wide occuring every 16.7 ms.

Figure 2-7 Synchronization and Blanking

when the electron beam reaches the right-hand side of the CRT, and the beam is reset back to the left hand side by the monitor.

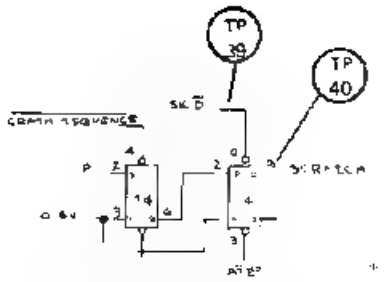
2-33. H RESET resets the sync counters after 451 clock pulses or counts. This is the end of the line (which actually occurs in the middle of the screen) so the counters must be started again. Horizontal blanking (H BLANK) is initiated by H RESET and lasts for 32 clock pulses. During this time information to be displayed on the next line is loaded into many parts of the PCB. The final horizontal sync signal (H SYNC) is composed of both H RESET and H BLANK and tells the electron beam when to start and stop its sweep.

2-34. Vertical reset serves the same purpose as H RESET except it occurs after 521 horizontal blanking pulses or half lines) when the electron beam is in the lower right hand corner of the CRT. There is no vertical blanking signal because no information needs to be loaded during vertical reset. The vertical sync signal serves the same purpose as H SYNC except it is timed to the vertical operation of the monitor.

2-35. The sync signals are generated in the following manner (see Figure 2-7). The clock starts L2 counting, and when L2 reaches TC (terminal count), TC goes high and stays high for one clock pulse. Since TC of L2 is connected to CEP (count enable parallel) of K2, when TC of L2 goes high, K2 is advanced by one count by the clock pulse at pin 2. K2 then counts 15 clock pulses and then TC of K2 goes high (after a total of 255 clock pulses). The falling edge of the 256th clock pulse causes K1-3 to go high and it will stay high until the 451st clock pulse when it is reset by H RESET. This 256H is divided again at K1-5 producing the 512th clock pulse or count which is the line that divides the CRT in half.

2-36. H RESET is an output of H1 and it is created by the addition of 256H, 128H, 64H and 2H and the result of J1-8 is a pulse 2H wide and 450 clock pulses from the last H RESET pulse. This is clocked through H1 by CLOCK producing the H RESET signal. Horizontal blanking is generated by H RESET which sets the RS flip-flop composed of the F1 gates. This causes H BLANK to go high and 32 clock pulses later it resets the RS flip-flop producing a blanking pulse 32 clock pulses wide after the H RESET pulse. Horizontal blanking is then gated with $\overline{\text{H RESET}}$ and $\overline{\text{512H}}$ to produce H SYNC.

2-37. Vertical reset is generated by horizontal blanking which clocks counter F3 at pin 14. The counter divides the clock frequency by eight and the output of this counter goes to H2 where it is again divided eight times. The result



TP 39	LOGIC PROBE	High until brake switch is closed, then drops low
	OSCILLOSCOPE	Same as Logic Probe
TP 40	LOGIC PROBE	Low going high when brake switch is closed
	OSCILLOSCOPE	Same as Logic Probe

Figure 2-8. Screech Logic

ing signal is finally divided another four times by counter J2. J2 is allowed to divide only to four (a count of 512) because on the 521st count (512 plus 8V plus one more H RESET pulse) all the counters are reset by V RESET. Vertical sync is created by RS flip-flop which is set by V RESET and reset by 8V. This produces a high sync pulse which is four lines wide.

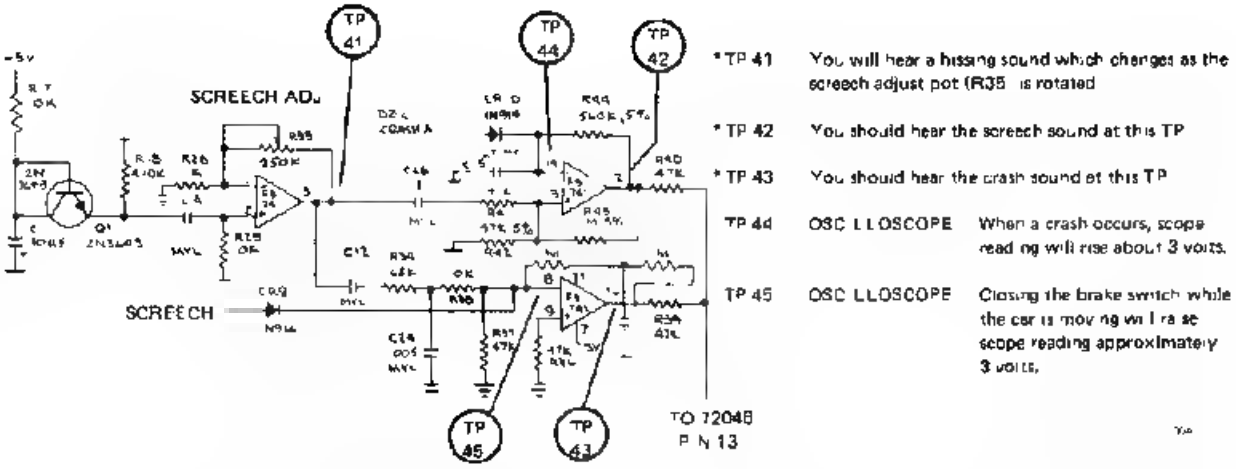
2-38. Because there are an odd number of half-lines being counted out, the electron beam must start at the center of the top of the screen every other field to achieve vertical reset. This is why the first line of the even field begins in the center of the CRT.

2-39 SCREECH LOGIC

2-40. This circuit (see Figure 2-8) generates the SCREECH signal, which creates the "screech" sound through the screech sound generator and through the 8103 of the speed control circuit. $\overline{\text{ATTRACT}}$ must be high (a game started) to enable the screech circuit. If $\overline{\text{SKID}}$ (the "brakes applied" signal) goes low presetting flip-flop C1 the SCREECH signal will go high. When SKID returns high 1024V will be clocked through two frames later turning the SCREECH signal off.

2-41 SCREECH AND CRASH SOUND GENERATION

2-42. This circuit creates the screech and crash sound signals which eventually wind up in the audio amplifier where they are amplified so that they can be transformed into audible sounds by the speaker. The screech sound occurs when the brakes are applied (while the car is moving



*NOTE To check test po nts 41 43 make a noise probe by connecting your video probe from capacitor C8 (in audio amp circu t) to TPs 4 43 f you hear the o lowing sounds the sound generator s O K although ad ustmen of R35 may be ndicated. Volume of noise probe TPs may be adjusted with the volume pot

Figure 2-9 Screech and Crash Sound Generator

and the crash sound resu ts from a coll sion between the car and any one of the race course py ons Both signals go through the 8103 hybrid before reach ng the aud o amp f er

2-43. Refer to Figure 2-9 Transistor Q1 is the actual noise generator and the s gnal from Q1 is amplif ed by F9-3. Trim pot R35 var es the feedback threshold of amp f er F9 wh ch l mits the number of "noise spikes" a owed through F9-3, thereby adjusting the qua ty of the screech and crash sounds When the brake switch s c osed and the car is moving, SK D is enal led SKID presets f p flop C1 in the screech logic and the SCREECH output at pin 9 goes high When SCREECH goes high, the crash sound opera tional amplifier is shut off at F9 8 allowing only the screech sound to reach the 8103. The screech sound is always being generated except when disabled by CRASH A If a crash occurs, CRASH A goes high wh ch disab es the screech amp f er at F9-14 a owing only the crash sound through to the 8103

2-44 ENGINE RPM SOUND GENERAT ON

2-45. Th s circu t creates the sounds of the car eng ne both when t s idling and when t is moving. This is accom pl shed w th three function generators and one e ectronic attenuator See F gures 2-10 and 2-11

2-46. When ATTRACT s h gh (dur ng the attract mode) Q3 conducts and ho ds pins 5 of C8, D8 and E8 above ground potential disab ng these function generators When a game s started, ATTRACT drops low and these function generators are enab ed Clos ng the gas pedal switch drops the RPM signal voltage from 0 volts to about 4 volts which causes the function generators to modu ate the frequencies of the r signa s

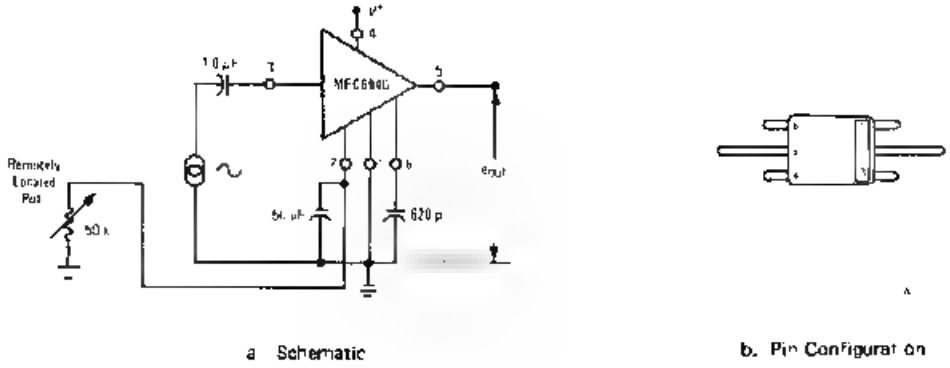
2-47 The sound signals from C8 and D8 are the inputs to the attenuator (F8), and the signal from E8 modulates the amplitude of the attenuator output The resu ting sound signa s carried to the audio amp f er and then to the speaker Note that each 566 function generator is n d v dual y adjustable by trim pots R60 R55, and R50 See F gure 2-11 for adjustment details

2-48. THE AUDIO AMPLIFIER

2-49. An aud o amplifier is necessary to drive the speak er See F gure 2-12. The sound signals enter the amp f er circu t through R16 and C8. The res stance of R4 deter mines the ga n (the vo ume) and is adjusted by turn ng the small blue trim pot (marked "volume") found near the LM 380 The LM 380 is a trans stor operated device which amplifies the sound signal to a eve high enough to dr ve the speaker

2-50. SPEED CONTROL

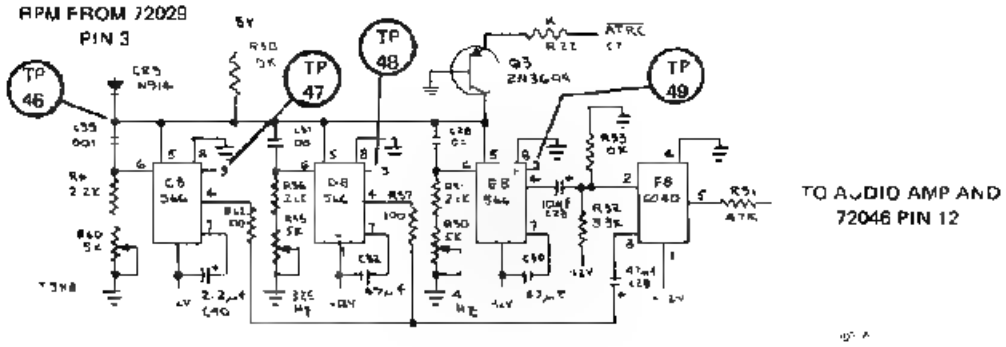
2 51 This c rcuit uses three custom ch ps (8103, 8098 and 8099) wh ch have been specifica ly designed for Gran



a. Schematic

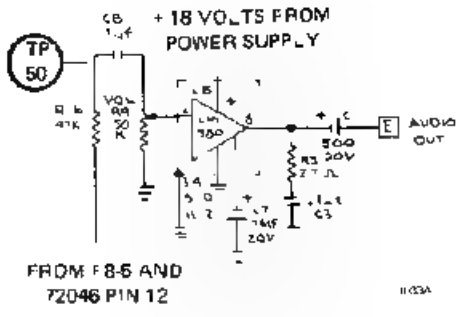
b. Pin Configuration

Figure 2-10 Electronic Attenuator



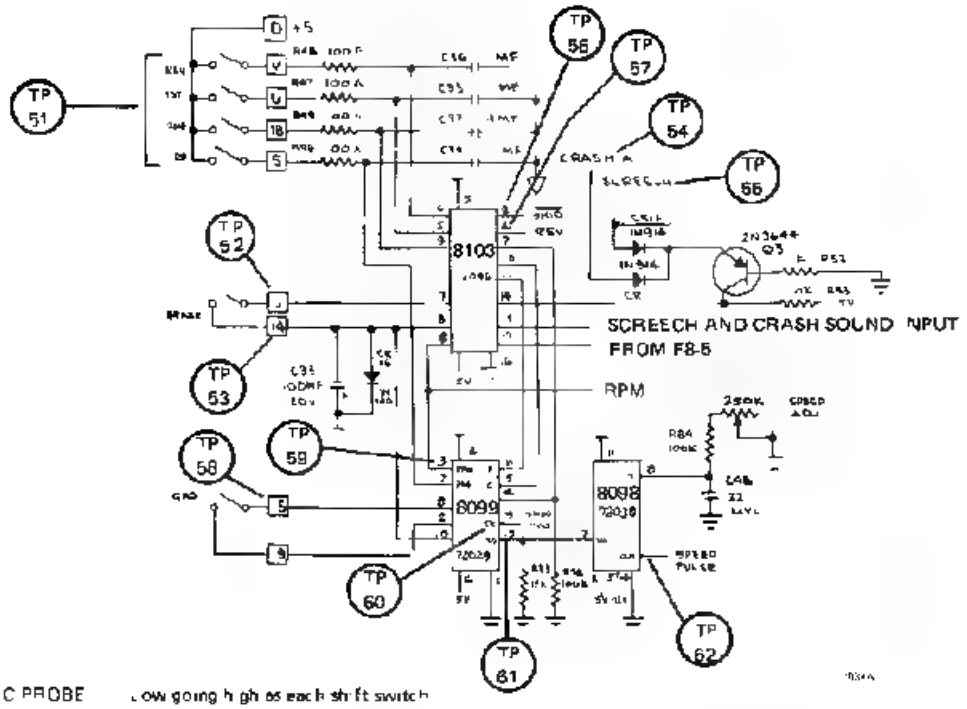
TP 48:	OSCILLOSCOPE	When R55 is correctly adjusted, you will see a 3.07 ms square wave.	TP 46	OSCILLOSCOPE	Closing the gas pedal switch causes the RPM signal voltage to drop from 0 to -4 volts.
TP 49	OSCILLOSCOPE	When R50 is correctly adjusted, you will see a 7.42 ms square wave.	TP 47	OSCILLOSCOPE	When R60 is correctly adjusted, you will see a 13 ms square wave.

Figure 2-11 Engine RPM Sound Generator



TP 50 Use the "noise probe" method to test the audio amplifier. Turn the volume down, attach the clip end of a video probe to capacitor C8 and run the prod down the vertical sync counter outputs. You will hear a series of tones from counter pins H2-12, 9, 8 and 11.

Figure 2-12. The Audio Amplifier



TP 51 LOGIC PROBE — Low going high as each shift switch is closed

OSCILLOSCOPE — Same as Logic Probe.

TP 52 OSCILLOSCOPE — 5 volts rising to + 2 volts when the brake switch is closed or a crash occurs.

VTVM — Same as Oscilloscope

TP 53 Check voltage drop with the Oscilloscope or voltmeter as you reach top speed in each gear

Reverse	0.8 volts
1st gear	0.8 volts
2nd gear	1.7 volts
3rd gear	3.5 volts

TP 54 LOGIC PROBE — Low going high when a crash occurs.

OSCILLOSCOPE — 0 volts rising to + 3.5 volts at crash

VTVM — Same as Oscilloscope

TP 55 LOGIC PROBE — Low going high when brake switch closed.

OSCILLOSCOPE — 0 volts rising to + 3.5 volts when brake switch is closed.

TP 56 LOGIC PROBE — High going low when brake switch is closed

OSCILLOSCOPE — Same as Logic Probe

TP 57 LOGIC PROBE — High going low when gearshift is in reverse

OSCILLOSCOPE — Same as Logic Probe.

TP 58 Check with Oscilloscope or voltmeter. Voltage should drop from + 5 volts to the indicated values as you reach top speed in each gear.

Reverse	+ 2.5 volts
1st gear	+ 2.5 volts
2nd gear	+ 2.5 volts
3rd gear	+ 4.3 volts

TP 59 Check with Oscilloscope or voltmeter. Voltage should drop from 0 volts to the indicated values as you reach top speed in each gear

Reverse	- 3.7 volts
1st gear	- 3.7 volts
2nd gear	- 3.8 volts
3rd gear	- 4.3 volts

TP 60 LOGIC PROBE — Low when car is at rest, high when car crashes.

OSCILLOSCOPE — Same as Logic Probe.

TP 61 Check with Oscilloscope or voltmeter. Voltages should drop from 0 volts to indicated values as you reach top speed in each gear

Reverse	- 0.5 volts
1st gear	- 0.5 volts
2nd gear	- 1.2 volts
3rd gear	- 2.6 volts

TP 62 LOGIC PROBE — Low when car at rest, low and pulsing when car is moving.

OSCILLOSCOPE — Following readings are to be taken with car at top speed in each gear

Reverse	58 ms between pulses.
1st gear	58 ms between pulses.
2nd gear	35 ms between pulses.
3rd gear	16 ms between pulses.

Figure 2-13. Speed Control

Trak 10 and are available only through Atari, Inc. If one of these chips should fail, order a replacement by the part number on the chip itself. The speed control circuit controls the car speed, the engine RPM sound and the screech and crash sounds. Refer to Figure 2-13 for the following discussion.

NOTE

Schematic chip numbers 8103, 8099 and 8098 correspond to actual chip numbers 72046, 72029 and 72030.

2-52. **8103/72046 Input/Output Conditions.** When any one of the shift switches is closed, the line connected to that switch goes high. Three of these switches (reverse, 1st and 2nd) are connected to pins 5, 6 and 9 of the 8103, and the 3rd gear switch is connected to pin 7 of the 8099. Closing these switches eventually controls the SPEED PULSES output from the 8098 as you will see under the discussion of the 8098.

2-53. The screech and crash sound signals enter the 8103 at pin 13. Pin 12 is the sound output. When the brake pedal switch is closed, SKID (pin 2) goes low and the SCREECH signal goes high. SCREECH disables the crash sound generator which allows only the screech sound through to the 8103. The screech sound is enabled through the 8103 by the closing of the brake switch, and continues to come out until capacitor C33 completely discharges through pin 17.

2-54. When a crash occurs, CRASH A goes low disabling the screech sound and allowing only the crash sound to reach the 8103. Both the screech and the crash sounds are controlled by the input to pin 14 which rises from -5 volts to +2.5 volts if you crash or step on the brake. So when a crash occurs, only the crash sound is enabled through the 8103. REV (reverse) at pin 4 goes low whenever the reverse shift switch is closed. This signal goes to C2-9 (steering encoder circuit) and then to the ROM address multiplexers to control the direction of the car image.

2-55. **8099/72029 Input/Output Conditions.** Pins 2 and 8 of the 8099 are connected to the gas pedal switch and control the acceleration of the car. When the car is stationary or in gear with no gas, pin 8 will be +5 volts. When you step on the gas, this will drop to approximately 2.4 volts in first and second gears and rise to 4 volts in third. Pin 2, on the other hand, is at 0 volts when the car is stationary or in gear with no gas. When in first or second gear with the gas switch closed, pin 2 will rise to about +2.4 volts and will rise to 4 volts in third gear with the gas pedal depressed.

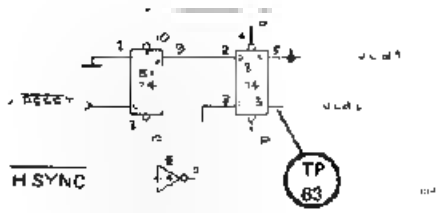
2-56. Pin 3 (RPM) is at 0 volts when the gas switch is open and drops to about -3.8 volts when you step on the gas in first. When you shift into second, pin 3 rises to approximately -2 volts and then drops to about -3.8 volts as the car picks up speed. When you shift into third it rises to -2 volts again and drops down to about -4.2 volts when the car reaches maximum speed. Top speed in reverse should produce about -3.8 volts at pin 3.

2-57. Pin 13 is the input to the 8098 Speed Pulse Generator. Pin 13 starts at 0 volts and drops to -0.5 volts at top speed in first gear. When you shift into second it rises to about -2 volts and drops to about -3.8 volts as the car picks up speed. When you shift into third it rises to -2 volts again and then drops down to about -4.2 volts when the car reaches maximum speed. Closing the reverse switch causes pin 13 to drop from 0 volts to -0.5 volts.

2-58. **8098/72030 Input/Output Conditions.** As pin 7 of the 8098 drops lower and lower, the speed pulses from pin 1 increase in frequency. This frequency is adjustable by the SPEED ADJUST pot R84 (see Section 1 for more details on this adjustment). The input to pin 9 of the 8099 comes from D5-8 (the crash circuit) and is used to disable the speed pulses during the attract mode or during a crash. This pin must go high to disable.

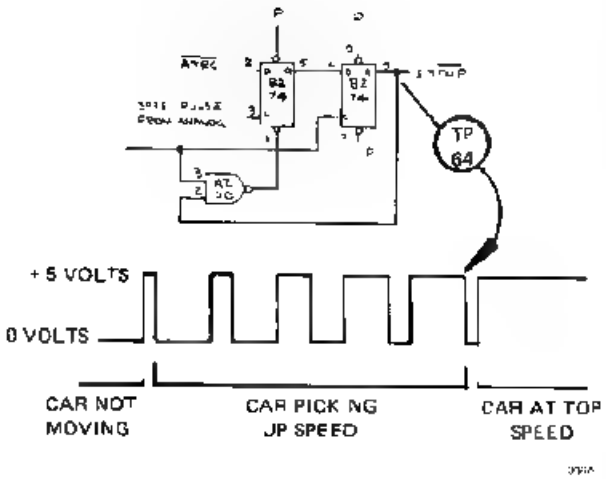
2-59. **VLd1**

2-60. VLd1 (vertical load one) is used to address the ROM for the vertical positioning of the car image. Refer to Figure 2-14. $\overline{V\ RESET}$ clocks the low from B1-12 out the Q output and this low waits at B1-2 until it is clocked through by $\overline{H\ SYNC}$. The Q output (B1-5) presets B1-9 causing a high to appear at B1-9. This high is clocked through to B1-5 on the next H SYNC pulse. The result is a VLd1 pulse which occurs once per field and is one H SYNC pulse wide.



TP 83	LOGIC PROBE	Low and pulsing.
	OSCILLOSCOPE	High pulse 63.5 ms wide occuring every 16.7 ms.

Figure 2-14. VLd1

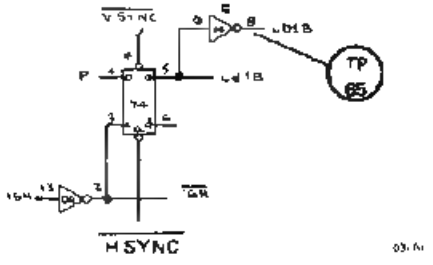


TP 64 LOGIC PROBE — Low when car at rest.
Low and pulsing when car is accelerating.
High when car reaches top speed in 3rd gear (provided speed pot is adjusted correctly)
OSCILLOSCOPE — See waveform above

Figure 2-15. 1 STOP

2-61 1 STOP

2-62 This signal is a ROM address which determines the speed with which the car image is moved. The input to this circuit (see Figure 2-15) is SPEED PULSE from pin 1 of the 8088 in the speed control circuit. As the car picks up speed, the speed pulses increase in frequency. When the car is stationary, 1 STOP is low. As the car starts moving 1 STOP begins pulsing high and the pulses get closer together and longer in duration until the car reaches top speed in third gear, at which time the signal stays high.



TP 65 LOGIC PROBE — Low and pulsing.
OSCILLOSCOPE — High pulse 5 ms wide occurring every 63.5 ms.

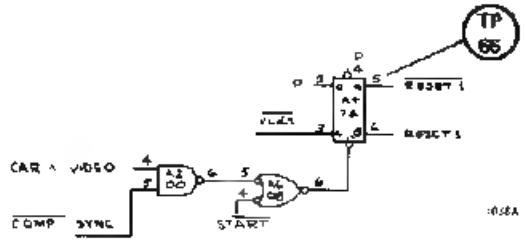
Figure 2-16. Ld1B

2-63 Ld1B

2-64 Ld1B (load one B) is another ROM address, however, it is also used in several other places to load information into counters, etc. See Figure 2-16. H $\overline{\text{SYNC}}$ clears flip-flop D1. Sixteen clock pulses later, the high is clocked from the D input out the Q output and is inverted to become Ld1B. $\overline{\text{V SYNC}}$ disables this function once per field, producing a wider Ld1B pulse.

2-65. RESET 1

2-66. The function of this signal is to tell the car motion circuits where to reposition the car image at the start of a new game or after the car is driven off the race course. When CAR 1 VIDEO encounters $\overline{\text{COMPOSITE SYNC}}$ (i.e., the car is driven off the screen) A2-6 goes low causing a low to appear at A6-6 and this low clears flip-flop A4. The flip-flop remains cleared until it receives the next $\overline{\text{VLd1}}$ pulse which clocks the high from A4-2 out A4-5 and this signal is known as RESET 1. $\overline{\text{START}}$ serves a similar function in the circuit as the low from A2-6 in that it also clears RESET 1.



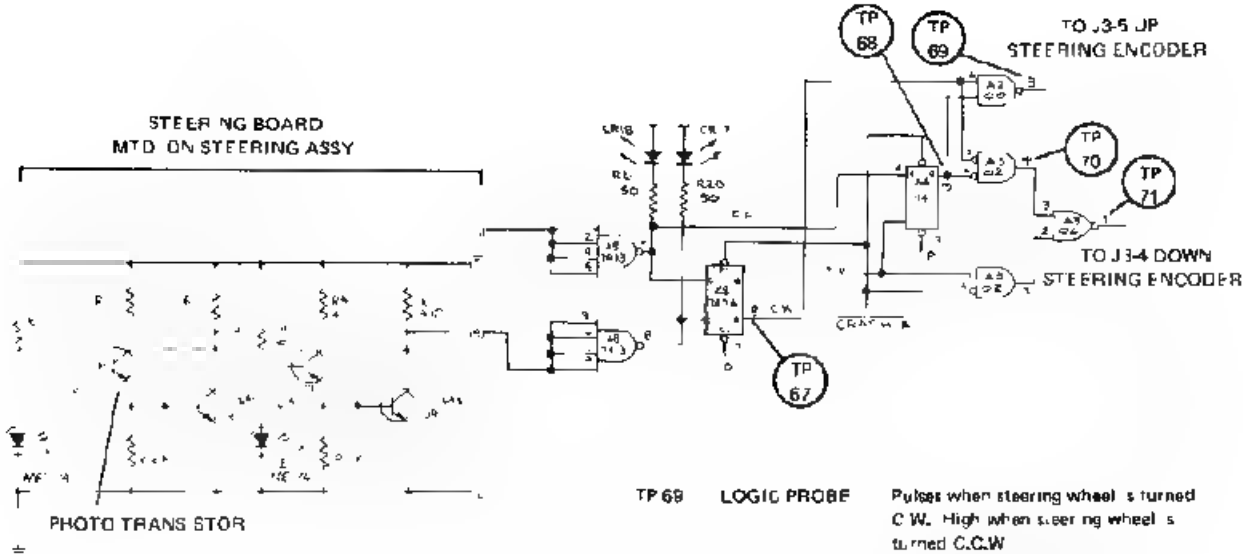
TP 66 LOGIC PROBE — Low pulse when the game starts or the car is driven off the track.
OSCILLOSCOPE — Same as Logic Probe.

Figure 2-17. RESET 1

2-67 STEERING CONTROL

2-68. The Steering Control circuit is shown in Figure 2-18. The two infrared light emitting diodes (LEDs) mounted on the steering assembly PCB are aimed directly at the two phototransistors and, as the slotted steering ring rotates, the path of light is broken up causing the phototransistors to pulse in a way which corresponds to the direction of the steering wheel rotation. These pulses are fed into four-input Schmitt triggers (J8) which clean up the pulses so the flip-flops can be triggered consistently.

2-69. When the steering wheel is turned in a clockwise direction a rising edge occurs at the clock input of K8 before a rising edge reaches the D input. This causes the CW



TP 67	LOGIC PROBE	High when steering wheel is turned C.W. Low when steering wheel is turned C.C.W.
	OSCILLOSCOPE	Same as Logic Probe.
TP 68	LOGIC PROBE	Pulses when steering wheel is turned and pulse rate rises as wheel is turned faster
	OSCILLOSCOPE	Same as Logic Probe.
TP 69	LOGIC PROBE	Pulses when steering wheel is turned C.W. High when steering wheel is turned C.C.W.
	OSCILLOSCOPE	Same as Logic Probe
TP 70	LOGIC PROBE	Pulses when steering wheel is turned C.C.W. Low when steering wheel is turned C.W.
	OSCILLOSCOPE	Same as Logic Probe.
TP 71	LOGIC PROBE	High except when steering wheel is turned C.C.W. or when a crash occurs.
	OSCILLOSCOPE	Same as Logic Probe

Figure 2-18 Steering Control

clockwise signal to be high, which enables gate A2 to advance the steering encoder discussed below and the steering encoder rotates the car in a clockwise direction. However, if the steering wheel is rotated in a counterclockwise direction, a rising edge will occur at the D input before a rising edge reaches the clock input. This produces a low CW signal.

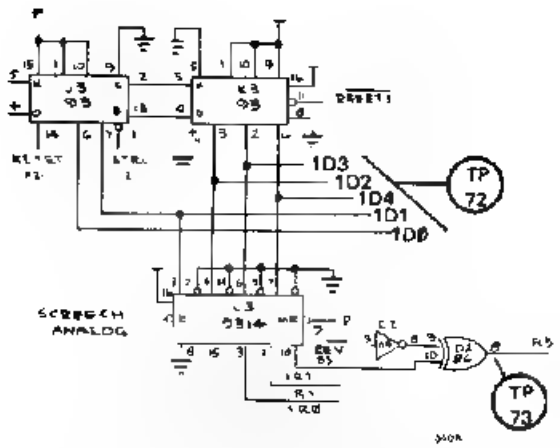
2-70. The rate signal is clocked through A4 by 128V. If RATE and CW are high, the rising edge of 128V clocks a high out A4-9 and the counters of the encoder are incremented (advanced). If RATE and CW are both low on the rising edge of 128V, A3 will decrement the counters and the car image will be rotated in a counterclockwise direction.

2-71. During a crash, $\overline{\text{CRASH}}$ A goes low which presets K8 producing a low CW. It also presets A4 producing a high at A4-9 which shuts off gate A3. This allows A3 to pass 128V decrementing the encoder counters and thereby causing the car image to spin uncontrollably during the crash.

2-72. Two LEDs (CR17 and CR18) have been included on the main PCB to facilitate troubleshooting the steering assembly. The pulses from the Schmitt triggers light the LEDs. If the LEDs flicker as you rotate the steering wheel, the steering assembly components are probably OK and the malfunction is most likely located in another part of the steering circuitry. If the LEDs do not flicker, look for foreign material between the infrared LEDs and the phototransistors of the steering PCB, physical damage to the steering assembly, broken connections or a malfunctioning Schmitt trigger.

2-73. THE STEERING ENCODER

2-74. The steering encoder directs the ROM to read out the different aspects of the car image as the steering wheel is rotated. See Figure 2-19. The steering control circuit decides whether to pulse the UP (U at J3-5) or the DOWN (D at J3-4) line of the J3 up-down counter. As the UP input is pulsed, a binary code results at output pins 6 and 7 of J3. After 15 pulses into the UP input, a carry pulse is produced



TP 72.	LOGIC PROBE	Changes state twice per each complete car image revolution.
	OSCILLOSCOPE	Same as Logic Probe.
TP 73.	LOGIC PROBE	The signal from L3 10 will change state when REV goes low.
	OSCILLOSCOPE	Same as Logic Probe.

Figure 2-19 Steering Encoder

at J3-12. This advances K3 which then produces another binary code at its output pins 2, 3, and 6. However, if the DOWN input to J3 is pulsed, J3 will count down from the last loaded number and, when it reaches 0, a borrow pulse is generated at J3-13 which decrements K3.

2-75. At the beginning of the game, or if the car is driven off the track, $\overline{\text{RESET 1}}$ goes low. This resets the counters to zero and re-orients the car image. L3 is a latch which takes the 1D1, 1D2, 1D3 and 1D4 outputs from the counters and passes these signals on to the ROM multiplexers unless SCREECH is high. A high SCREECH latches up the last information from the counters and holds it until SCREECH goes low again. This causes the car image to continue moving in the same direction it was going when the brakes were applied, even if the steering wheel is turned which produces a realistic "slide" or "drift".

2-76. REV at C2-9 selects and inverts the most significant digit from L3, causing the car to back up in the opposite direction the car image was oriented in when the gear shifter was placed in reverse. This is necessary to produce a realistic back-up sequence.

2-77 CRASH AND PLAYTIME

2-78. This circuit has several functions. (1) it generates the crash signal when the car is driven into the pylons, (2) it times the length of the game, and (3) it incorporates the TEST switch which is used to turn off the playtimer and crash mode when testing the board. See Figure 2-20 for the following discussion.

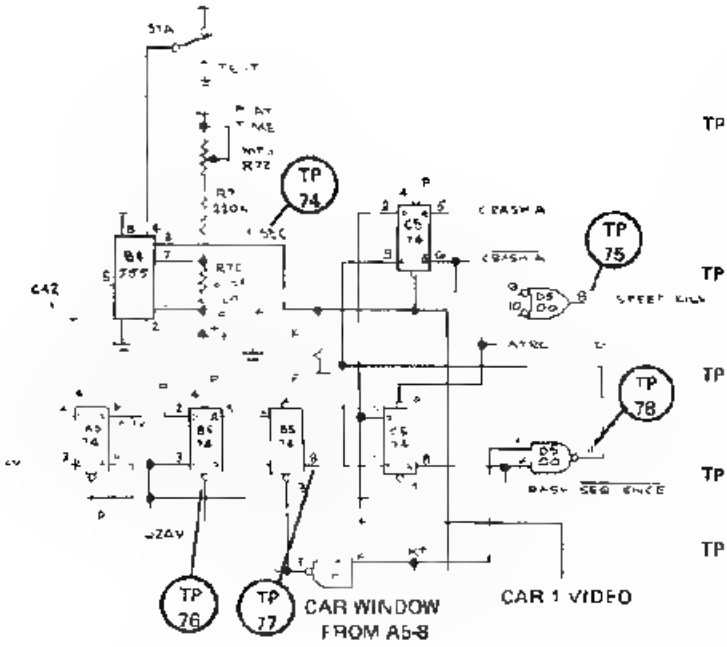
2-79. The 555 timer at B8 is the component which actually provides the timing. The amount of time it takes to charge C43 determines the pulse width out of the 555, and controls the period of time the output signal 1 SEC is high. R72 adjusts both the crash time period and the playtime by varying the amount of time required to charge the capacitor. The timer output is used to clear the crash flip-flops after a crash has occurred. It is also the input to the game timer circuit which turns the game off after it counts a certain number of 1 SEC pulses. If the TEST switch is in the normal position, the 555 is allowed to produce the high 1 SEC pulses. However, if the switch is set to the TEST position, pin 4 of the 555 is grounded out and the game timer cannot count down.

2-80. This circuit also generates the crash signal (CRASH A) whenever the car window encounters the race track signal by gating the two signals together at D5-3. A crash produces a low at D5-3 which clears both B5 flip-flops and 2048V later, a low is clocked out B5-8. During the time B5-8 is high, flip flop C5 is enabled and asks the question, "is there a car on the pylons?" If the answer is "no" (i.e., one of the wheels has just barely glanced off a pylon), C5 continues to repeat the question until it is cleared at pin 13 by a low from B5-8. However, if the answer to C5's question is "yes" C5-8 goes low causing D5-11 to go high and the "yes" information is latched into C5 at pin 5 producing a high at CRASH A and a low at $\overline{\text{CRASH A}}$. A low $\overline{\text{CRASH A}}$ produces a low SPEED $\overline{\text{KILL}}$ signal from D5-8 which stops the car motion. A low $\overline{\text{ATRC}}$ will also produce a low SPEED KILL and stop the car whenever the computer is in the attract mode.

2-81 THE MEMORY CIRCUIT

2-82. This circuit stores information which is later read out for the generation of the car image, the race track display and the score and timer displays. The main components are four multiplexers and one 16K ROM which has been specially programmed for Gran Trak 10 (See Figure 2-21).

2-83. The ROM is a memory unit which stores binary information. This information is read out of the ROM by the multiplexers, and these outputs go to other circuits where the information is used to form the different aspects



TP 74.	LOGIC PROBE	High with low pulses approximately once per second when TEST switch is in the play mode. Frequency of 1 SEC is adjustable by R72.
	OSCILLOSCOPE	Same as Logic Probe.
TP 75	LOGIC PROBE	High going low when the car crashes
	OSCILLOSCOPE	Same as Logic Probe.
TP 76	LOGIC PROBE	Drops low when the car encounters the race track.
	OSCILLOSCOPE	Same as Logic Probe.
TP 77	LOGIC PROBE	High pulse when the car crashes.
	OSCILLOSCOPE	Same as Logic Probe.
TP 78	LOGIC PROBE	Normally high, low and pulsing, changes to high when a crash occurs.

Figure 2-20 Crash and Playtime

of the car image, the race track display etc. The ROM stores 2048 eight bit words. Multiplexers select certain signals from a larger input of signals and these output signals are the "addresses" for the ROM. A different multiplexer address is required to read out each different eight bit ROM word. For example, when information is needed for the generation of the car image, the multiplexers select the correct ROM address and this selected signal reads out the desired car image information from the ROM. This ROM information is then fed into the car motion circuits and a new aspect of the car image is displayed on the CRT.

2-84. It is important to understand how the multiplexers function, so we have included a brief discussion of basic multiplexer operation. Figure 2-22 is the schematic of a basic two input two-to one data multiplexer. When the data select line (S) is high, the signal at the A input is reflected at the output. When S is low, signal B appears at the output and not A. The multiplexers used to address the ROM are nothing more than elaborations of the foregoing theme. The ROM requires multiplexers which can select one of two four-bit words.

2-85. The ROM itself is not a particularly complicated device, it is useful only because it can store so much information in a small space. You can visualize the ROM being constructed from 2048 rows of 8 diode gates each, where each gate is connected to one of the eight ROM outputs. Each diode in every row is specially programmed so that it reads out either a high or a low when it is addressed. Each row of eight gates must be addressed by a different binary number. Since there are 2048 rows the ROM requires a ten-bit address input. When this number is read out by the multiplexers into the ROM address input, each diode in the selected row reads out its high or low to one of the ROM outputs.

2-86. **Troubleshooting the Memory Circuit:** Some typical symptoms of malfunctions in this circuit are a distorted or missing car image, portions of the race track distorted or missing or distortion of the lap counter or game timer displays. If you suspect trouble in this section, the first step is to replace the ROM. A plug-in type receptacle has been provided to facilitate replacing the ROM. If the malfunction disappears, leave the new ROM in. However, the ROM failure rate is extremely low, so if a new ROM does not fix the problem, go on to the following troubleshooting procedures.

2-87. If the ROM is OK, next check the ROM addresses at ROM inputs A^0 A^9. If these addresses are not OK, check the inputs to the multiplexers, the multiplexed outputs and any gating which may be between the multiplexer outputs and the ROM inputs. The ROM address table (Table 2-1) is invaluable in troubleshooting this section. We will use a car image problem to demonstrate the use of the address table. To find the correct address for the car image at the ROM inputs look under the column labeled "CAR A". Then clip the scope probe to the device the ROM information is to be read into, which is shift register F6. The

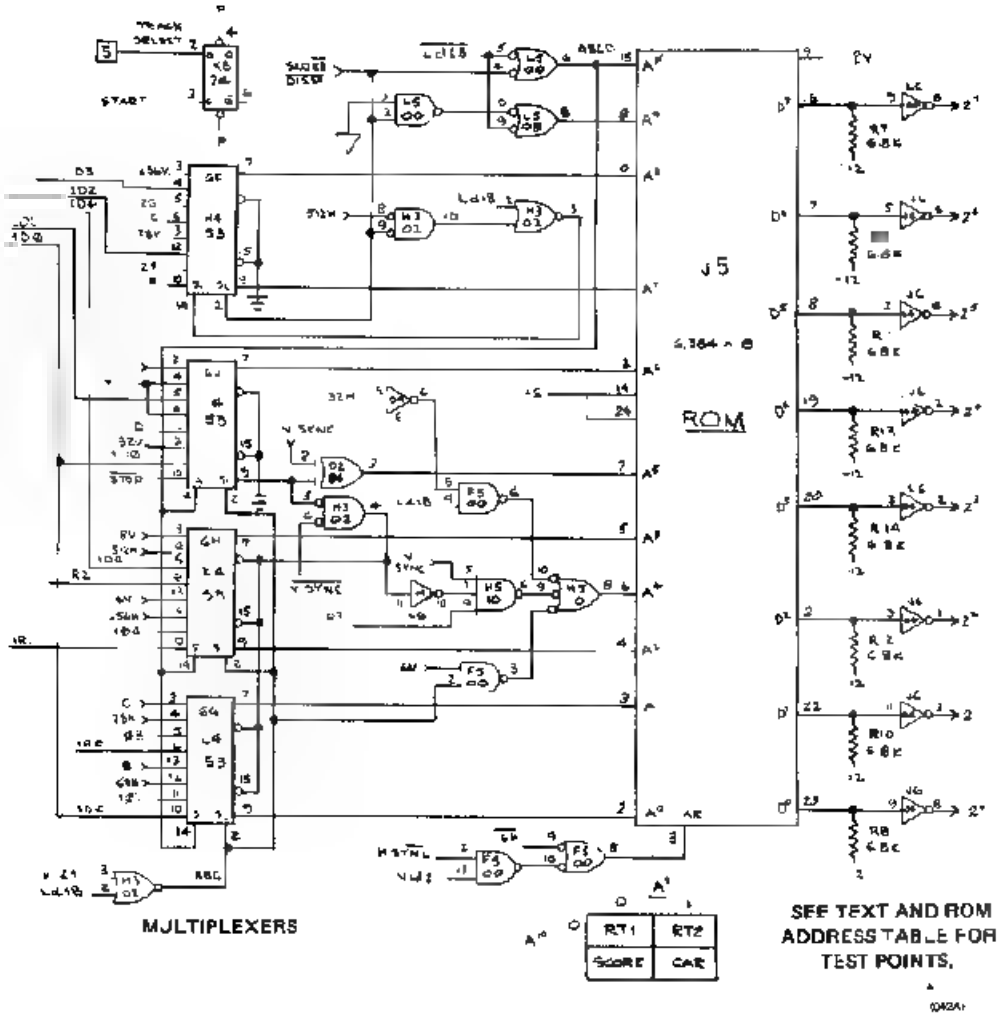


Figure 2-21 The Memory Circuit

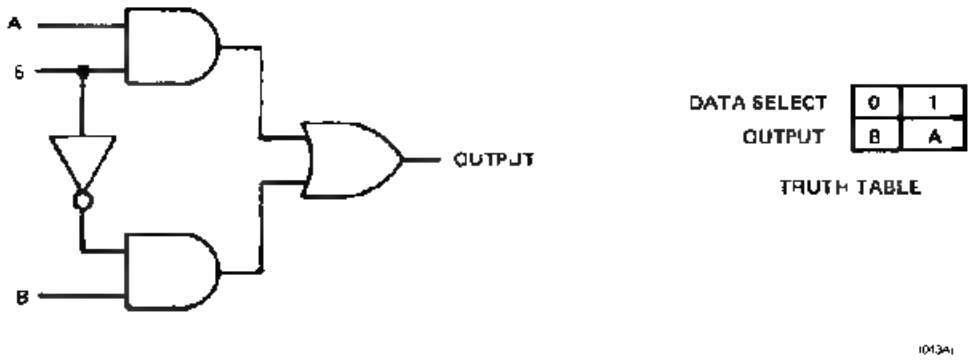


Figure 2-22. Basic Two Input Two-to-One Multiplexer

Table 2-1 ROM Address Table

CAR A	SCORE C	TIME D	1 PT E	2 PT F	SPEED CODE G	ROM ADD	MULTIPLEX ADD
1	1	1	0	0	0	AØ	
1	0	0	0	1	1	9	
1D3	1G	2G	256V	256V	256V	8	A+C+D+EFG
1D2	1F	2F	128V	128V	128V	7	A+C+D+EFG
1D1	1E	2E	64V	64V	64V	6	A+C+D+EFG
1DØ	1D	2D	32V	32V	0G0 1 STOP	5	A+C+D+EF+G
$\overline{32H}$*	16V	16V	16V	16V	1R3 0 STOP	4	A+C+D+EF+G
1D4	8V	8V	512H	512H	1R2	3	A+CD+EF+G
104	4V	4V	256H	256H	1R1	2	A+CD+EF+G
103	1C	2C	128H	128H	1RØ	1	A+C+D+EF+G
102	1B	2B	64H	64H	1DØ	0	A+C+D+EF+G

* 32H=1 FIRST PART OF CAR
0 SECOND PART OF CAR

probe would be placed on the pin which is used to control when the data will be entered. In this case, it is the shift load input ($S/\overline{L}$) at pin 1. When the shift load pin goes low, the information will be loaded into the register. Then take the second probe and check the ROM address inputs and compare these with the information at the multiplexer inputs. Finally, compare all of this information with the table.

2-88 For example, first check ROM address $A^{\emptyset}$ (pin 15) with the second probe and you should see a high pulse occurring at the same time as the low shift load pulse. Note that this correctly corresponds to the ROM address table. Then look at A^{9} (pin 8, and again there should be a high pulse occurring simultaneously with the low shift load pulse. Now go to A^{8} and you should see signal 1D3 which will pulse high and low as the steering wheel is rotated. Continue to check all the address inputs in the same fashion. If you find some information which does not correctly correspond, start checking back through the multiplexers and gates (if any). If all the information checks out OK, examine the component that information is being loaded into (shift register F6 in this case).

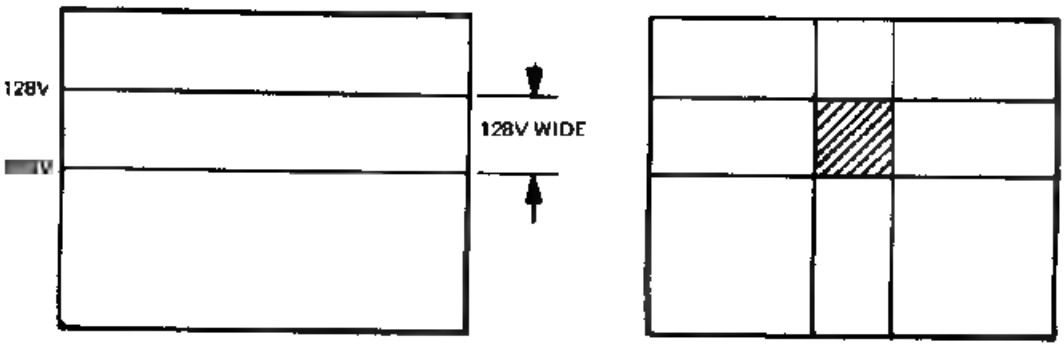
2-89 To troubleshoot the multiplexers, first check the multiplexer inputs. If any of these do not check out, go to the section which produces the malfunctioning signal and locate the malfunction there. However, if all the multiplexer inputs are OK, check the data select lines by going to gates H3 and L5 and verifying the presence of the correct Ld1B, VLd1, 512H and SCORE DISP inputs. If all of the data select inputs are also OK, you must check the multiplexers themselves.

2-90 The multiplexers are most easily checked using a logic comparator (see paragraph 1.11). The comparator will yield fast and accurate results. If you do not have a comparator, use the following procedure. First tie both multiplexer select lines low and look at the information from pins 7 and 9 (multiplexed outputs) which must match the inputs at pins 6 and 10 (multiplexer inputs). If OK, tie S_1 high and S_2 low, and pins 7 and 9 should match 5 and 11. If OK here, tie S_1 low and S_2 high, and 7 and 9 should equal 4 and 12. To check the last set, tie both select lines high and pins 7 and 9 should match 3 and 13.

2.91 THE WINDOW CONCEPT

2.92 After the video signals are generated by the computer, they must be displayed on the desired part of the CRT. This is done by directing the signals to appear only within a certain area or "window". The key idea behind the window concept is that of limits or boundries.

2.93 Your video probe is a test instrument which can be used to display the windows directly on the CRT. To see a graphic display of windows, attach one probe clip to the negative (-) side of the video coupling capacitor (C44) and



a. Horizontal Window b. Complete Window

Figure 2-23. CRT Windows

run the other end across the sync counter outputs. You probably noticed, as you ran the probe across the vertical sync outputs, that the resulting windows were horizontal in appearance. The most confusing part of the window concept is the fact that it takes vertical signals to define a horizontal window and vice versa.

2-94. Examine Figure 2-23a and notice the vertical signal 256V which defines a horizontal line approximately half way down the CRT. Since the raster is composed of 521 half lines (or 260.5 whole lines), the signal 256V "tells" the electron beam to modulate its scan at the 256th half line down from the top of the screen and the lower half of the screen is white. This is why it takes a vertical signal to define a horizontal line a certain vertical distance down the CRT. If we create a similar line, except 128 half lines down the CRT, the result will be a band 128 half lines wide bounded at the top by 128V and at the bottom by 256V. This band is known as a horizontal window.

2-95. A complete window (Figure 2-23b) is created by generating a similar vertical window and gating the two windows together, so that we have an area with all four sides defined. The video signals are gated with the window so that they can only appear when the window occurs. The result is that the video can then only appear within the window.

2-96. INTRODUCTION TO MOTION

2-97. The illusion of car motion is achieved by rapidly shifting the car image in the same way the illusion of motion is created on the motion picture screen by the film in the projector. The eye perceives this image shift as motion because of a phenomenon known as "retinal after image". The last seen image is "remembered" for a short time and as the position of the image is shifted a number of times in rapid succession, the eye "overlaps" the images and perceives the shifting process as continuous motion. Since the TV monitor has a frame rate of 30/second it is possible to shift the car image so rapidly that the eye is completely fooled.

2-98. The speed or velocity of the car image is determined by the shift-rate/frame-rate ratio. If the image is shifted once every frame it will appear to move much faster than if it were shifted only once every three frames. The direction of the image is controlled by varying the rate at which the car image windows are shifted with respect to each other. Notice the vertical motion window in Figure 2-24a. As this window moves up and down, the image contained within it also moves up and down. Figure 2-24b shows the horizontal motion window which controls how the image is shifted from left to right. When the two windows are combined, the image can be vectored at any angle by individually varying the rate each window is shifted.

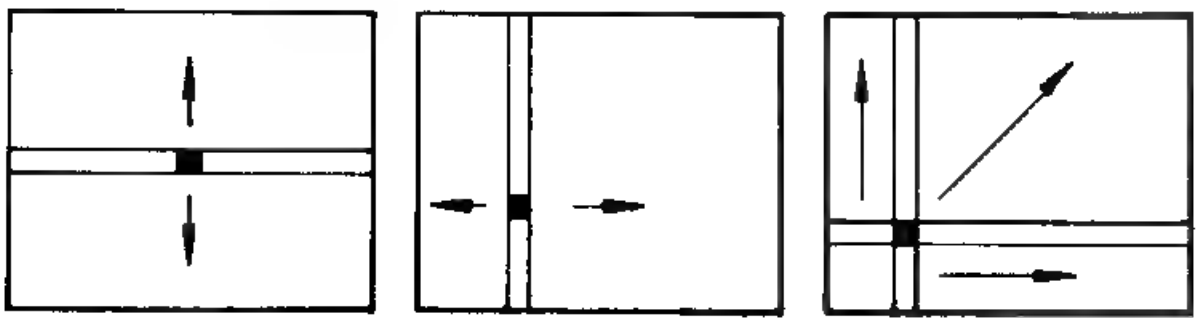


Figure 2-24. CRT Image Motion

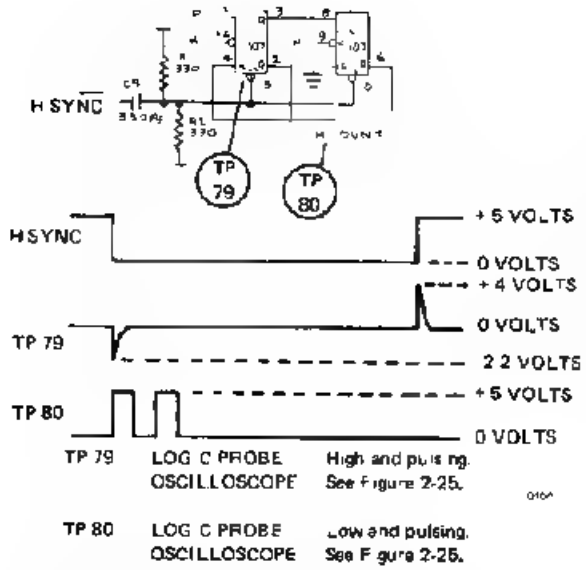


Figure 2-25. Horizontal Count

2-99 The speed of the image is controlled by shifting the window with respect to sync. If the window frequency is the same as sync, it will be displayed in exactly the same place during each TV frame and it will appear stationary. However, if the window is generated a little slower or faster than sync, it will be shifted a certain amount each frame and will appear to move. This is done by entering different binary codes at the parallel inputs to the 9316 counters of the motion circuits. The stop code is that binary number which times the window with sync and therefore stops motion. Other codes cause a change in this relationship and the window is shifted with respect to sync.

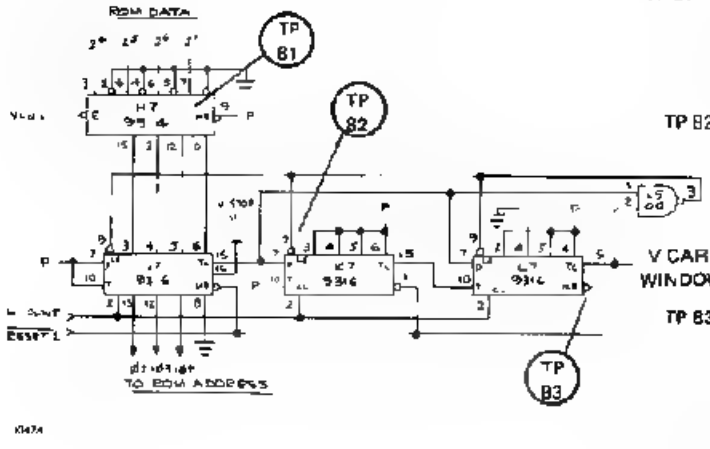
2-100 HORIZONTAL COUNT

2-101 H COUNT is used to clock counter J2 (vertical positioning for the car image) twice per line. See the circuit in Figure 2-25. Capacitor C9 and resistors R1 and R2 create a very short reset pulse for both L1 flip-flops and this produces a high at both Q outputs. On the first 1H pulse, the $\overline{Q}$ output at L1-2 goes low while L1-3 goes high. The Q at L1-6 remains unchanged. On the second 1H pulse, L1-2 goes high and L1-6 goes low. On the third 1H pulse, both L1-2 and L1-6 go low and stay low until both flip-flops are again reset by the capacitor and resistors.

2-102 VERTICAL CAR MOTION

2-103 The vertical car motion circuit is shown in Figure 2-26. When $\overline{VLd1}$ is high, the ROM data is latched into H7 and appears at the outputs when $\overline{VLd1}$ drops low again. This information is loaded into the parallel inputs of J7 when the line from L5-3 goes low. It takes 4096 H COUNT pulses to produce a low on this line. The counters start counting from the last number loaded in by L5-3 and count 4096 H COUNT pulses at which time a new number is loaded in.

2-104 The stop code for vertical motion is 3575 (1 1 1 0 1 1 1 1 1/1 0 1 1). When this number is entered into the counters, car motion ceases (4096 minus 3575 equals 521 which is the sync frequency). However, as the least significant digits of the stop code are changed, the 9316s begin their count from a different number and the resulting car window frequency is changed. For example, if the number 0 1 1 0 is loaded into J7, the window will move down at

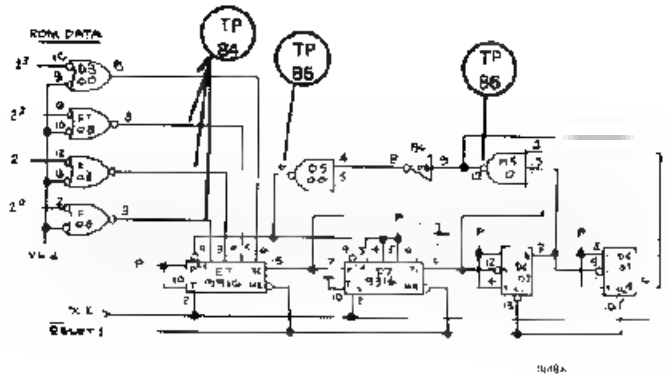


TP 81 Hold pin 1 of H7 low. Then using the Oscilloscope or the Logic Probe, check to see if the input signals at pins 3, 4, 6 and 7 are reflected at output pins 15, 13, 12 and 10. NOTE: CRT images break up when you hold VLd1 low.

TP 82: To check counters, first look at pin 9 with the Video Probe and you should see a thin black line which moves with the car and is parallel to the bottom edge of the CRT. Then hold pin 9 low successively and check to see if the input signals of each counter (pins 3, 4, 5 and 6) are reflected at the outputs (pins 13, 12, 11 and 8).

TP 83: VIDEO PROBE At this test point, you will see the vertical car motion window which will appear as a white horizontal band.

Figure 2-26. Vertical Car Motion



TP 84 Hold VLd1 low. This should generate the stop code 0-0-0-1 at pins 3, 4, 5 and 6 of E7. Then hold pins 9 of E7 and D7 low and the stop code should be reflected at output pins 14, 13, 12 and 11 of E7 and D7.

TP 85 VIDEO PROBE Thin black vertical line which moves with the car image.

TP 86 VIDEO PROBE The video probe will reveal the horizontal car motion window which will appear as a black band moving with the car image.

Figure 2-27. Horizontal Car Motion

the slowest velocity (4096 minus 3574 equals 522 which is slightly faster than sync). Notice the RESET 1 line which resets the car image at the start of the game or after the car has been driven off the track.

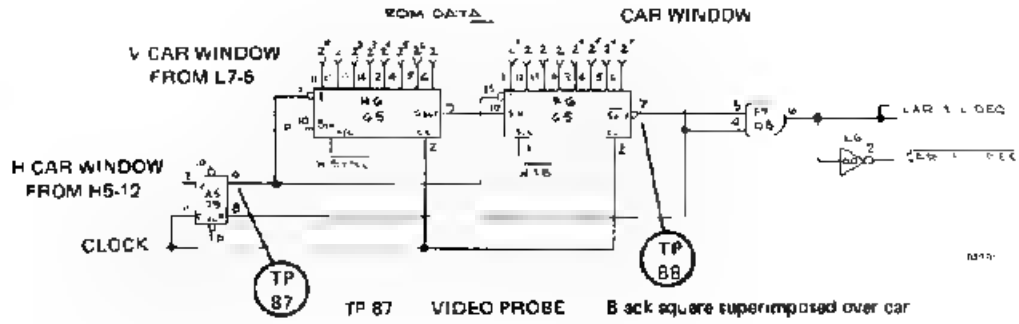
2-105. HORIZONTAL CAR MOTION

2-106. The only real differences between the horizontal and vertical motion circuits are that the horizontal counters are clocked by CLOCK rather than H COUNT and that different numbers are loaded into the counters. See Figure 2-27. VLd1 is normally low and goes high once per field. During the time VLd1 is low, the stop code 0-0-0-1 is loaded into E7. When VLd1 goes high the ROM data is entered into E7 causing the horizontal motion window to shift.

2-107. CAR DISPLAY

2-108. The car display circuit uses both the outputs of the ROM and the outputs of the car motion circuits to generate the different aspects of the car image. The ROM supplies the necessary information for the car images, the car motion circuits move the car windows (and hence where the car image can appear) and the display circuit displays all this information on the CRT.

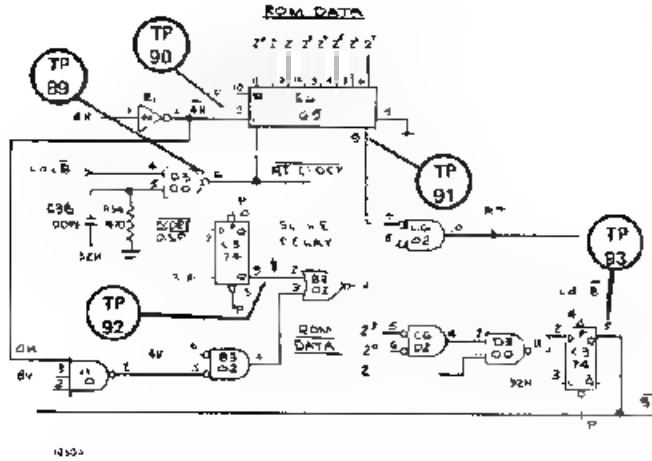
2-109. Refer to Figure 2-28. Since the data at the ROM outputs are in parallel form, a shift register is necessary to convert this parallel (simultaneously occurring) information to serial (sequentially occurring) information. This is necessary so the information bits can be loaded one after another to be displayed by the electron beam as it sweeps across



TP 87 VIDEO PROBE Black square superimposed over car image.

TP 88 VIDEO PROBE A number of horizontal white lines covering CRT from top to bottom. One or two of these lines intersect the car image and stop at the car

Figure 2-28. Car Display



TP 89	OSCILLOSCOPE	Low pulse 0.1 ms wide occurring every 4.5 ms except when Ld1B goes low.
TP 90	VIDEO PROBE	Vertical 4H bars covering screen from left to right. NOTE: Wider band in center is due to reset pulse.
TP 91	VIDEO PROBE	All race track windows visible.
TP 92	VIDEO PROBE	White windows over score and timer displays.
TP 93	VIDEO PROBE	Dark check point, finish line and non-delayed score and timer windows.

Figure 2-29. Race Track Display

the CRT. Two shift registers are needed because the car image is made up of 16 bits, and each shift register can only process 8 bits of information at a time.

2.110. The information is loaded at different times into the shift registers by $\overline{\text{H SYNC}}$ and Ld1B. When H SYNC and Ld1B both go low, one set of car information is loaded into H6 by H SYNC and the register latches up this information. When H SYNC returns high, Ld1B is still low and another set of car information is loaded into F6 and latched up when Ld1B returns high. As long as the clock inhibit (1) of a shift register is high, the information remains latched in the register. However, when input 1 goes low, the clock pulses at pin 2 read out the information serially. The clock inhibit goes low during the car window signal which comes from the Q output of A5. The car window is the intersection of the vertical and horizontal car motion windows. So when the inhibit inputs of the registers go low, F6 reads out its latched up information out pin 7 (the serial output) while H6 is simultaneously reading its information into F6. When all the information originally stored in F6 is read out, F6-7, F6 then reads out the information read into it by H6. All this information is gated with the car window at F7 to form CAR 1 VIDEO which is the final car image signal.

2-111. RACE TRACK DISPLAY

2-112. The information for the generation of the race track display is read out of the ROM and this data is loaded into the parallel inputs of shift register E6 by $\overline{\text{RT CLOCK}}$ (see Figure 2-29). $\overline{\text{RT CLOCK}}$ is created at D3 by the gating of Ld1B with the modified 32H signal. The rising edge of 32H charges capacitor C38 which discharges through R54, providing a very sharp high going spike (there is also a low going spike but since it is below threshold voltage it cannot enable D3 and only the high-going spike is passed). This signal is gated with Ld1B which allows only race track data to enter the shift register.

2.113. There are eight 4H pulses per each RT CLOCK pulse and the race track information is clocked out E6 9 serially by every 4H pulse. The resulting signal contains both the race track and the score information. Since the score window is generated at a different time than the score information is read out of the ROM, the score window (SCORE DISP) must be delayed at C3 by 32H so that the resulting score window occurs simultaneously with the score information and in the correct part of the CRT.

2.114. SPECIAL DATA prevents the race track data from being displayed when special information such as the finish line, the check points and the score need to be displayed. Otherwise race track images would be written over the special data. Whenever 2^0 and 2^3 go low and while 2^1 and $\overline{\text{Ld1B}}$ are high, the special data is clocked out 32H later.

2.115. The sizes of the pylons and the check points are determined by J1 and B3. This information is gated with SCORE DELAY at B3 and then with the race track and score information at C6 to form the complete race track signal (RT).

2-116. TIME AND SCORE STORAGE

2.117. The primary functions of this circuit are to count the number of laps scored and the amount of elapsed time

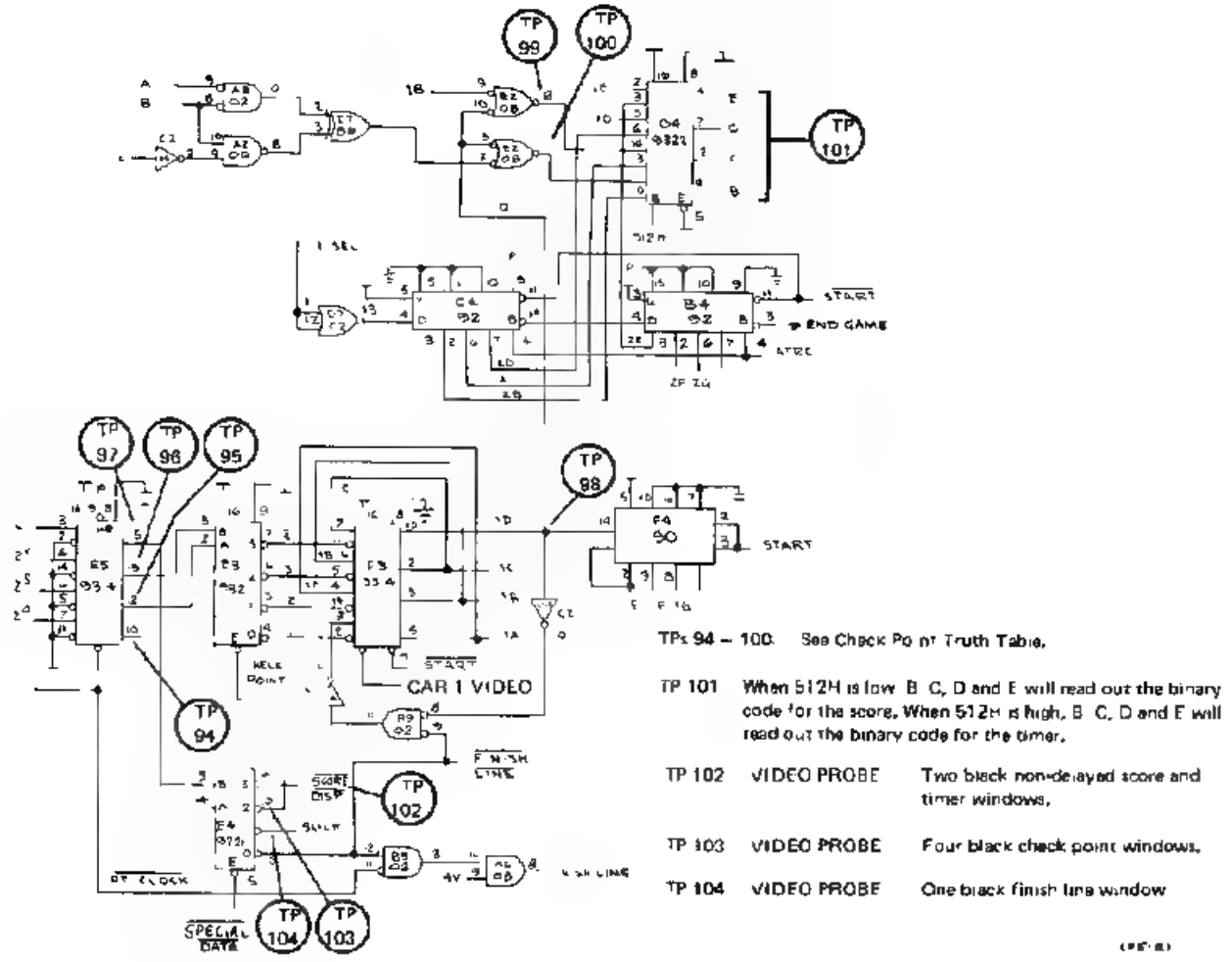


Figure 2-30. Time and Score Storage

Table 2-2 Check Point Truth Table

NO. OF CHECK POINTS PASSED	TP 94 E5 10	TP 95 E5 12	TP 96 E5 13	TP 97 E5 15	TP 98 1D	TP 99 D4 14	TP 100 D4 11
0	L	L	L	L	L	L	L
1	L	L	L	H	L	L	H
2	L	L	H	H	L	H	L
3	L	H	H	H	L	H	H
4	H	H	H	H	H	L	L

Laps are scored only by passing the race course check points in proper order. If the check points are passed correctly, the lap score is increased by an increment of two. The information needed for generating the score images is contained within the ROM and read out by the following process.

2-118. Refer to Figure 2-30. The ROM data at the parallel inputs of E5 are loaded into that latch when RT CLOCK goes low and is latched when RT CLOCK goes back high. The latched information enters the A and B inputs of the one of four decoders E3 and E4. The state of the E input controls the state of the selected output signal and the output signal is selected by the states of the A and B inputs. For example, if both A and B are low, output 0 will be selected and if E is low, the selected output 0 will also be low. If A is high and B is low, output 1 will be selected and if the E input is high, then output 1 will be high.

2-119. SPECIAL DATA (the signal from the race track display section which contains the data for score display, slick, finish line and the check points) is the E input to E4 and whenever SPECIAL DATA is low, the selected output of E4 will also be low. For instance, when the check point information is to be read out of the ROM, A will be low and B will be high which selects output 2 which will be low because E (SPECIAL DATA) is also low. Output 2 will then contain all the check point information which is then sequentially selected by E3.

2-120. Output 0 of E4 is the finish line signal; however, it is 64 clock pulses wide — too wide for a functional finish line so it is gated with RT CLOCK at B3. Since RT CLOCK is a spike of very short duration, the resulting finish line signal at B3-13 will also be of very short duration and appear as a thin line. This thin finish line is then chopped into segments by gating it with 4V at A6 to give it a "dotted line" effect.

2-121. Laps are scored only by passing course check points in the specified order and this is accomplished by selectively enabling latch F3. At the beginning of a new game, START goes high which clears F3 so it can accept new information. Clearing F3 produces lows at pins 15, 13, 12 and 10 (1A, 1B, 1C and 1D) and this causes lows to appear at pins 4, 6 and 7 and a high to appear at pin 3.

2-122. When the car passes through the first check point, the car signal at pin 1 will go high enabling the high at pin 3 to appear at pin 15 which goes around and holds pin 4 high. When the car passes through the second check point, the high at pin 4 will be enabled through to pin 13 and so on. This continues until the car has passed all the check points at which time 1D will go high incrementing counter F4 and

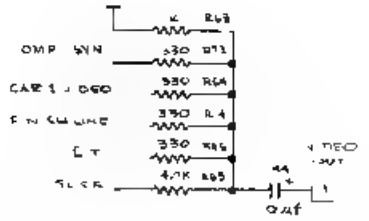


Figure 2-31 Video Summer

simultaneously returning a low to pin 3. A low at pin 3 forces a low to appear at pin 15 which goes around and causes pin 4 to be low which in turn causes pin 13 to be low. This continues until all the outputs are low and the latch is ready to record a new set of check point and car image intersections.

2-123. The information at 1A, 1B, 1C and 1D must be converted to a binary code by gates A2, A3, D2 and E2 so that multiplexer D4 can correctly address the ROM score image information. The truth table in Table 2-2 shows how this is accomplished.

2-124. D4 is a quad two-to-one multiplexer which selects either the score storage information or the game timer information. The signal is selected by 512H and the outputs of the multiplexer (B, C, D and E) become inputs to the ROM multiplexers. Basically these outputs tell the ROM what number to look up and read out for the score and timer images stored within the ROM. The ROM only stores 17 sets of number display information (1 - 7 in tens and 0 - 9 in ones) which limits the numbers which can be displayed for the score and game timer. The lap score will count up to 78 and the game timer counts down from 78.

2-125. C4 is the ones counter for the game timer and B4 is the tens counter. When START goes low, these counters begin counting down from the number loaded into the parallel inputs (78) and count down by twos. When both counters reach zero, a low "borrow" (or END GAME) pulse is generated which resets the game to the attract mode. The length of the game can be changed by varying the 1 SEC pulses (see Section 1). Longer pulses are counted more slowly by the counters and thus the total game length is longer.

2-126. VIDEO SUMMER

2-127. The video summer shown in Figure 2-31 is simply a resistor summing network which collects all the video signals generated on the PCB, adds them across R63 and accouples them to the TV monitor. The negative side of C44 is the point of connection for the video probe when troubleshooting.

Table 2-3. GRAN TRAK 10 PCB Parts List

ITEM	PART NO	QTY	DESCRIPTION
1	000872	Ref	P C Board Assembly
2	000873	Ref	Schematic
3	10101	8	Resistor 100 ohm, 10% 1/4 Watt
4	10102	11	Resistor 1K ohm, 10%, 1 4 Watt
5	10103	6	Resistor 10K ohm, 10%, 1/4 Watt
6	10104	1	Resistor 100K ohm, 10% 1/4 Watt
7	10151	2	Resistor 150 ohm, 10% 1 4 Watt
8	10221	3	Resistor 220 ohm, 10% 1 4 Watt
9	10222	3	Resistor 2.2K ohm 0%. 1/4 Watt
10	10224	1	Resistor, 220K ohm 10% 1/4 Watt
11	10331	9	Resistor 330 ohm 10%, 1 4 Watt
12	10332	1	Resistor 3 3K ohm 10% 1/4 Watt
13	10471	2	Resistor 470 ohm, 10% 1 4 Watt
14	10473	7	Resistor 47K ohm 10%, 1 4 Watt
15	10681	1	Resistor 680 ohm, 10%. /4 Watt
16	10682	9	Resistor 6.8K ohm. 10%. 1/4 Watt
17	10683	1	Resistor, 68K ohm 10%, 1 4 Watt
18	11102		Resistor, 1K ohm, 5%, 1/4 Watt
19	11104	1	Resistor 100K ohm 5%, 1 4 Watt
20	11105	3	Resistor, 1M ohm, 5%, 1/4 Watt
21	1153	1	Resistor, 15K ohm, 5% 1 4 Watt
22	11270	1	Resistor, 2 7 ohm 10% 1/4 Watt
23	11471	1	Resistor 470 ohm, 5% 1/4 Watt
24	11472	1	Resistor 4.7K ohm. 5% 1 4 Watt
25	11561	1	Resistor 560 ohm 5%. 1/4 Watt
26	11564		Resistor, 560K ohm 5%, 1/4 Watt
27	11820		Resistor, 820 ohm, 5%, 1/4 Watt
28	12102	1	Resistor 180 ohm, 10%. 1/2 Watt
29	19100	1	Resistor, 4 ohm, 10 Watt
30	19109	1	Resistor, 50 ohm, 5 Watt, 20% Wire Wound
31	22105	1	1M ohm Trim Pot
32	22107	2	250K ohm Trim Pot
33	22502	3	5K ohm, Trim Pot
34	22503	1	50K ohm, Trim Pot
35	30100	2	Capacitor, 100 pfd mica @ 100V
36	30331	1	Capacitor, 330 pfd mica @ 100V, 20%
37	32471	2	Capacitor, 47 mfd Mylar
38	32221	1	Capacitor, 22 mfd Mylar 10%
39	32502	1	Capacitor, 0047 mfd Mylar
40	32101	5	Capacitor 0 1 mfd Mylar
41	3410	20	Capacitor, 1 mfd, Ceramic Bypass
42	34102	4	Capacitor, 001 mfd Ceramic Disc
43	35102	1	Capacitor, 1.0 mfd @ 5V E ectrolytic, 10%
44	35103	3	Capacitor 10 mfd @ 6V Electrolytic
45	35222	1	Capacitor 2 2 mfd @ 10v Electrolytic
46	35254	1	Capacitor 250 mfd @ 6V Electrolytic
47	35472	1	Capacitor, 4 7 mfd @ 6V Electrolytic, 20%
48	35473	1	Capacitor, 47 mfd @ 6V Electro ytic
49	35503	4	Capacitor, 50 mfd @ 10V E ectrolytic, 20%
50	35504	1	Capacitor, 500 mfd @ 20 v Electrolytic
51	37000	1	Capacitor 8000 mfd @ 16V Electrolytic
52	37102	1	Capacitor, 220 mfd @ 25V DC E ectrolytic
53	37103	1	Capacitor, 100 mfd @ 20V Electrolytic
54	37104	1	Capacitor, 2000 mfd @ 25V Electrolyt c
55	39100	1	Capacitor, 100 mfd, Tantalum 20%

Table 2-3. GRAN TRAK 10 PCB Parts List (Continued)

ITEM	PART NO.	QTY.	DESCRIPTION
56	60000	1	DPDT Slide Switch
57	70000	3	2N 3643 Transistor
58	70001	4	2N 3644 Transistor
59	70004	1	2N 6193 Transistor
60	71000	10	1N 914 Diode
61	71001	4	1N 4001 Diode
62	71003	1	1N 100 Diode
63	71006	2	Diode, 2.5A
64	71009	1	SCR MCR106-1
65	71010	1	1N 5241 Zener Diode
66	72000	5	Integrated Circuit, 7400
67	72001	6	Integrated Circuit, 7402
68	72002	5	Integrated Circuit, 7404
69	72003	2	Integrated Circuit, 7410
70	72010	14	Integrated Circuit, 7474
71	72012	1	Integrated Circuit, 7486
72	72013	1	Integrated Circuit, 7490
73	72014	3	Integrated Circuit, 7493
74	72015	3	Integrated Circuit, 74107
75	72016	4	Integrated Circuit, 74153
76	72017	7	Integrated Circuit, 9316
77	72018	1	Integrated Circuit, 555
78	72019	1	LM 309 K
79	72021	3	Integrated Circuit, 566
80	72025	1	Integrated Circuit, 9322
81	72027	3	Integrated Circuit, 7408
82	72029	1	8099 Hybrid
83	72030	1	8098 Hybrid
84	72031	2	Integrated Circuit, 9321
85	72032	2	Integrated Circuit, 74192
86	72033	3	Integrated Circuit, 74165
87	72035	2	Integrated Circuit, 74193
88	72036	4	Integrated Circuit, 9314
89	72042	1	Integrated Circuit, MFC 6040
90	72046	1	8103 Hybrid
91	72048	1	Integrated Circuit, LM 380
92	72049	1	Integrated Circuit, 74S04
93	72050	1	Integrated Circuit, 7413
94	72052	1	Integrated Circuit, RC4136D
95	74186	1	Integrated Circuit, ROM
96	75100	2	Screw, 6-32 x 5/8, Pan Head, S.S.
97	75101	4	Washer, No. 6 Internal Star Lock Washer
98	75102	2	Washer, No. 6 Flat
99	75103	2	Nut, 6-32, Hex
100	80009	2	Light Emitting Diode
101	80086	1	24 Pin I.C. Socket
102	81001	1	Crystal
103	83104	1	Wakefield Heatsink
104	000854	1	P.C.B. Revision E
105	001091	Ref.	Modification Drawing, RT Assembly
106	10474	1	Resistor, 470K, 10%, 1/4 Watt
107	10472	1	Resistor, 4.7K, 10%, 1/4 Watt

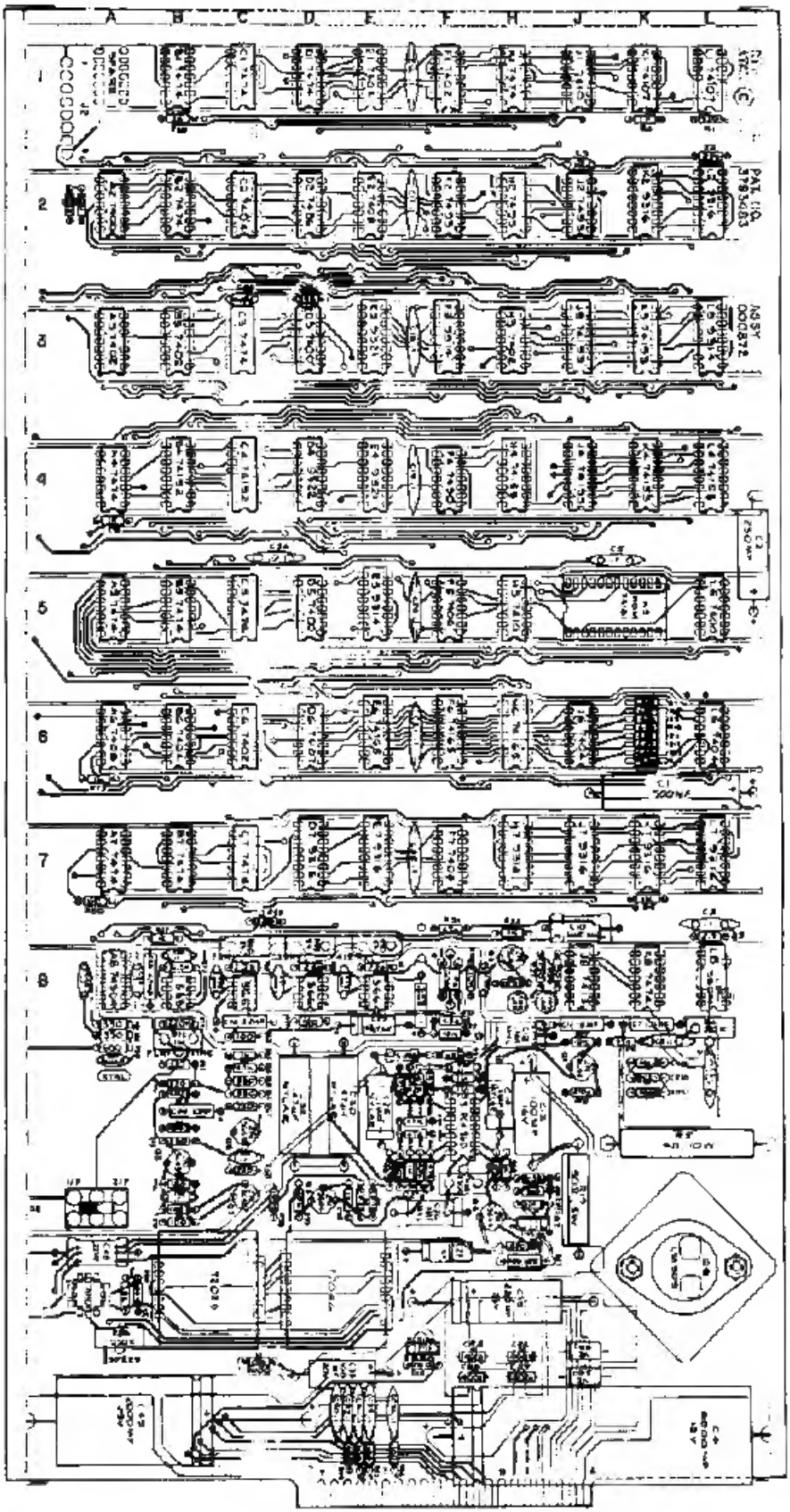


Figure 2-32. Computer Board Component Layout

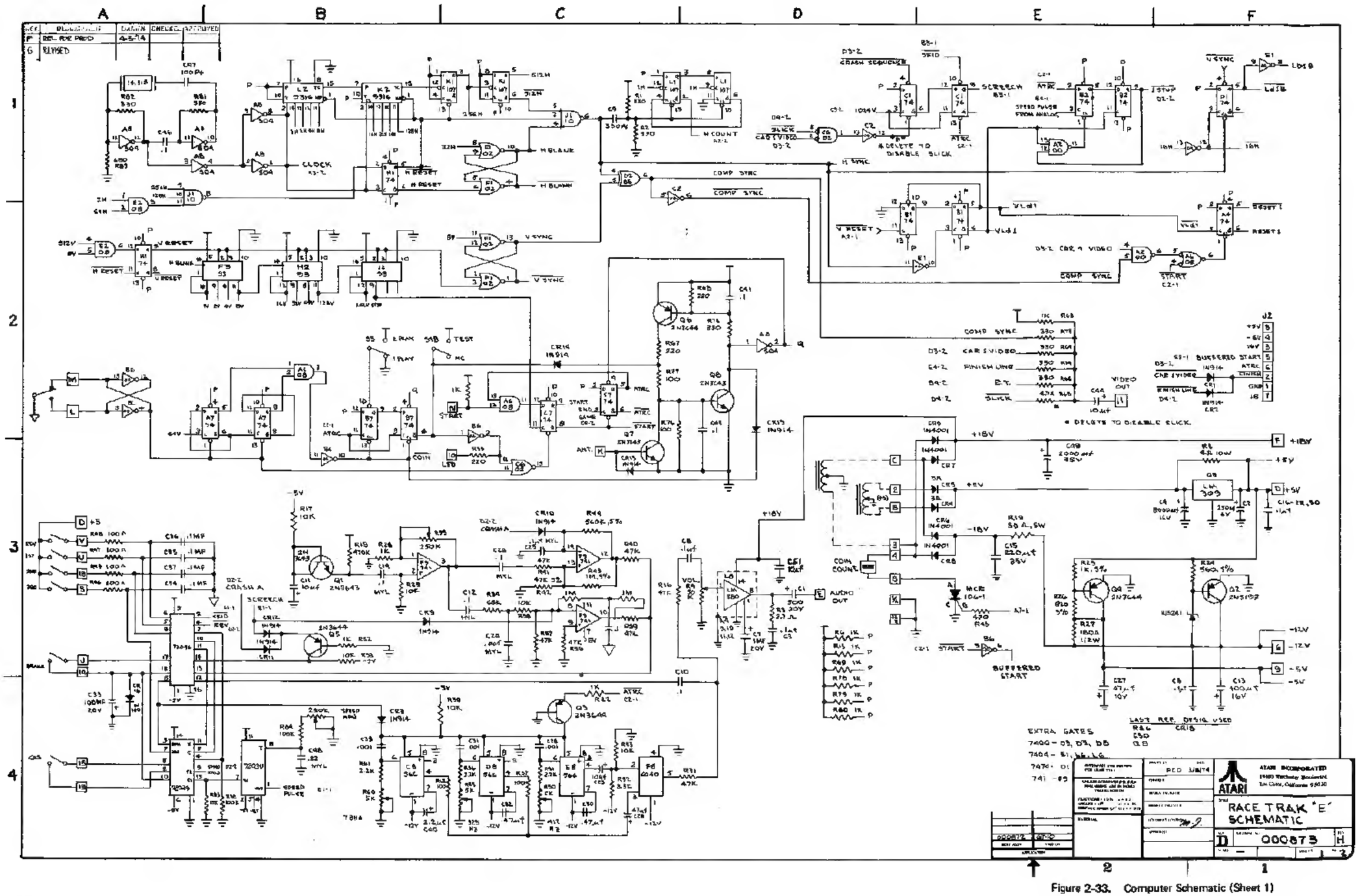


Figure 2-33. Computer Schematic (Sheet 1)

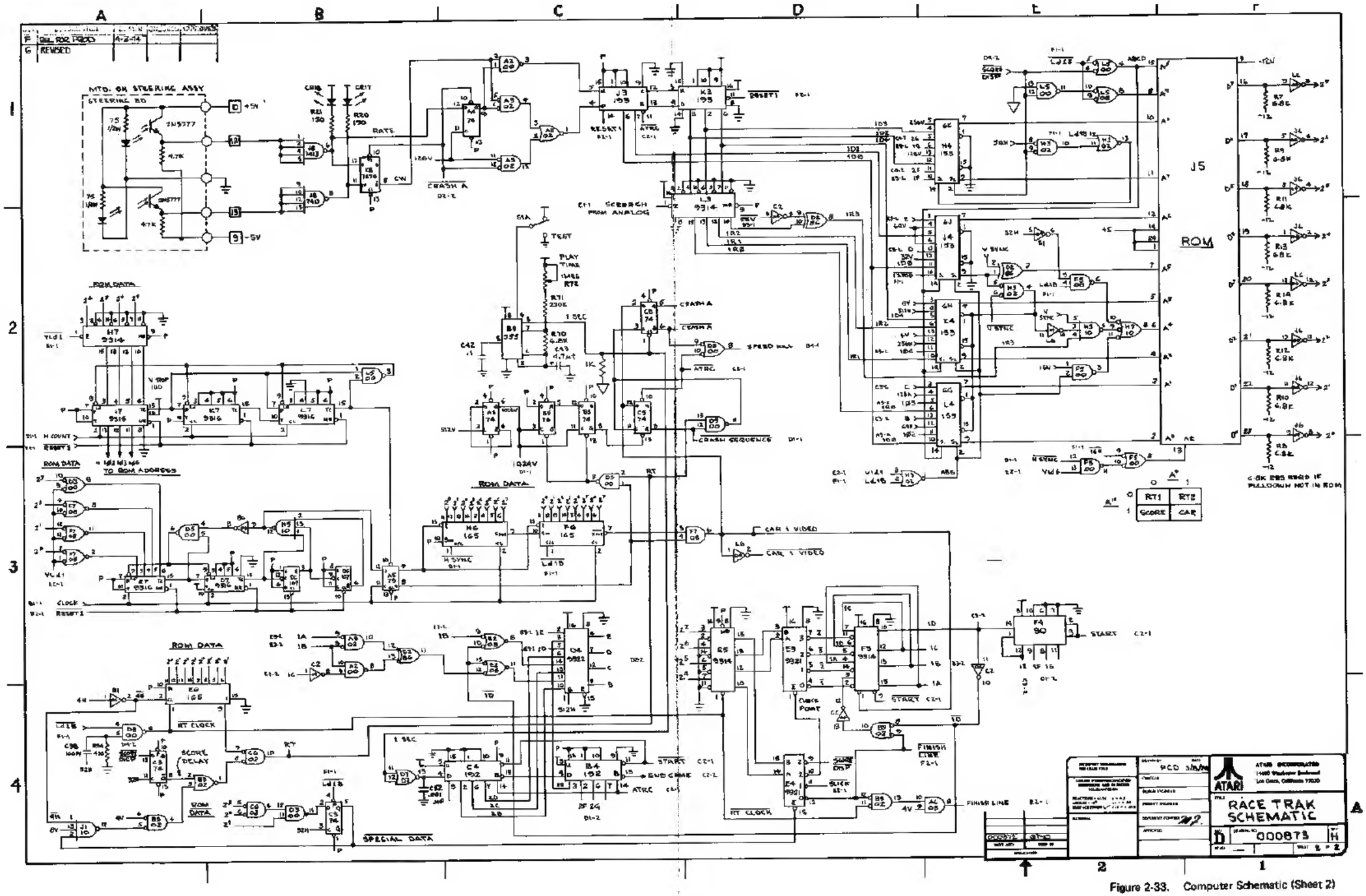


Figure 2-33. Computer Schematic (Sheet 2)